R-390A/URR DIGITAL FREQUENCY READOUT UNIT

(Interim Report)

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ABSTRACT

The design and development of the R-390A/URR Digital Frequency Readout Unit is presented in this report. The history of development including the techniques considered are discussed. Digital pulse subtraction, which was chosen as the most economical technique, is described in detail.

The new approach to frequency readout presented utilizes the existing local oscillators of the receiver and by a pulse subtraction process extracts the input frequency of the receiver with an accuracy of ± 20 Hz.

SECTION I

INTRODUCTION

1. STATEMENT OF THE PROBLEM

Communication receivers are generally operated in a very dense signal environment, especially in the lower frequency bands. To distinguish between stations operating at nearly identical carrier frequencies the receivers are provided with bandwidth select switches; however, the frequency readout from the receiver dial is not precise. A specific example is the R-390 receiver. From this receiver, frequency can be read to the nearest 200 Hz, but due to complicated tuner construction frequent calibration is necessary to maintain good accuracy. Calibration is a complex and time-consuming task and the receiver has to be taken out of operation during this procedure.

In tactical situations, it is often required to determine the exact frequency of the transmitter of interest. This cannot be accomplished with the R-390. To determine the frequency accurately, an auxillary digital readout unit is required.

2. PURPOSE OF THE TASK

The objective of this task was to design and construct a prototype model frequency readout unit and integrate it with the R-390A/URR radio receiver. Several techniques, which require the summing of receiver local oscillator frequencies, were to be investigated; and the optimum method was to be chosen in developing one prototype model. The main factors to be considered in the design were accuracy, reliability, size of the unit, ease of operation, and cost of construction. The unit should operate in real time without interrupting the incoming signal, providing digital frequency readout and a means for calibrating the receiver dial.

Two methods were chosen for investigation:

a. Single sideband technique of mixing to obtain frequency subtraction

b. Digital pulse elimination scheme

The unit was constructed utilizing the latter method.

SECTION II

FREQUENCY SUBTRACTION

GENERAL DISCUSSION

Band crowding in the field of HF communications has brought about the desirability of presenting the operator with an accurate readout of the frequency to which his receiver is tuned. Furthermore, it is undesirable to interrupt or degrade the signal of interest while determining the received frequency.

A logical method of achieving this is to use the information already contained in the local oscillators and the last IF. If one were to examine a particular double conversion receiver in detail he might find something similar to Figure 1.

The frequency of the final IF (f_{IF}) is expressed by equation (1):

$$f_{IF} = f_{LO_2} - (f_{LO_1} - f_{in}) \qquad (1)$$

f_{LO_x} = local oscillator frequency

Rearranging equation (1) and solving for f_{in} yields an expression for the input frequency f_{in}.

$$f_{in} = f_{LO_1} - (f_{LO_2} - f_{IF}) \qquad (2)$$

This equation indicates that the input frequency can be found by summing the local oscillators and the final IF frequency in the correct sequence. Essentially, the conversion process performed by the receiver must be reversed and the results counted and displayed.

Conventional techniques for subtracting two frequencies involve the use of mixers and some type of sideband suppression. Filters used must be narrow band and, therefore, tuned, making them expensive and cumbersome. Phase shift techniques of sideband suppression require wideband quadrature phase shifters and are unsatisfactory when used in conjunction with harmonically tuned oscillators.

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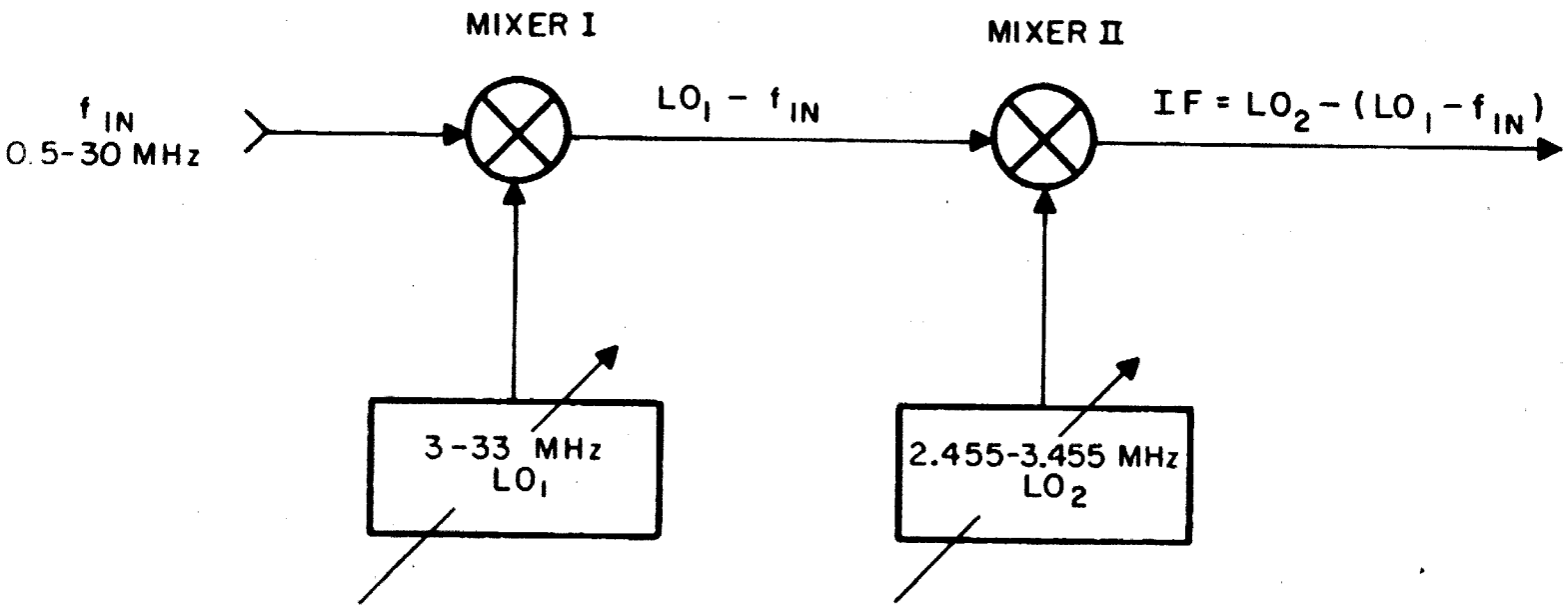

FIGURE 1 Block Diagram of a Particular Double Conversion Receiver (U)

Because of cost, it is highly undesirable to design the better part of a second receiver just to display the input frequency. Since the intended end is to display the input frequency, there appears to be no need to preserve pure sinusoidal waveforms if a counter is used to count pulses representative of the input frequency. .A digital technique seems made to order.

Again the necessary logic to directly satisfy the equation is costly and the time necessary to perform the subtraction makes this an unattractive solution. What is needed is a sequential subtraction that works in real time and is relatively simple. The answer lies in the development of a pulse subtraction technique. Two techniques were investigated and are described in the following sections.

2. FREQUENCY SUBTRACTION BY SINGLE SIDEBAND TECHNIQUE

The first method investigated was the use of a single sideband (SSB) technique of mixing to obtain the frequency subtraction. The process of subtraction may be represented by the equation:

$$f_{input} = \left[f_{LO_2} - (f_{LO_3}) \right] - f_{LO_1} \qquad (3)$$

f_{LO} = frequency of R-390A local oscillator

where each set of parentheses represents a frequency subtraction.

By using the SSB technique the necessity of a complicated filter network is avoided, provided that the input frequencies are relatively free of harmonics.

Figure 2 is a block diagram representing an SSB mixer. f_1 and f_2 are the two input signals; $f_1 - f_2$ is the output. The incoming signals are divided by a quadrature power splitter. The zero phase portion of both splitters are fed into a balanced mixer. Likewise, the quadrature phase portion of both splitters are fed into a second balanced mixer. The output of the two balanced mixers are summed to provide the SSB output E_o, the difference frequency $\omega_1 - \omega_2$

where

$$\omega_1 = 2\pi f_1$$

$$\omega_2 = 2\pi f_2$$

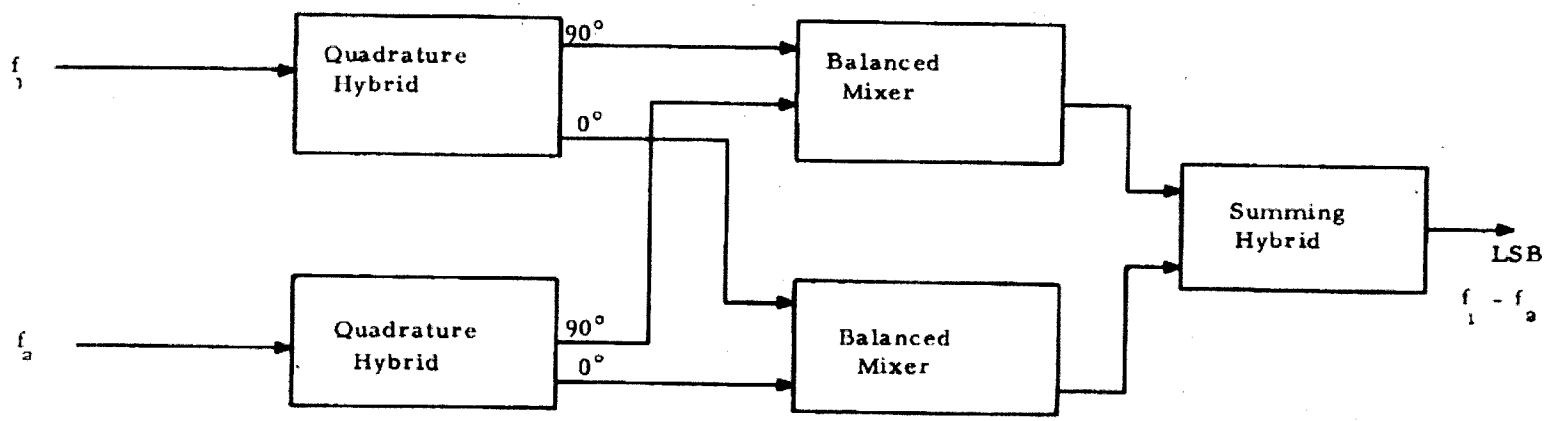

FIGURE 2 Single Sideband Mixer Block Diagram (U)

The output of mixer 2 is specifically represented by:

$$E_y = A_y \text{Cos } \omega_1 t + B_y \text{Cos } (\omega_1 + \omega_2)t + B_y \text{Cos } (\omega_1 - \omega_2)t \quad (4)$$

The output of mixer 1 is represented by:

$$E_x = A_x \text{Cos } (\omega_1 t + \phi) + B_x \text{Cos } [(\omega_1 t + \phi) + (\omega_2 t + \theta)] + B_x \text{Cos } [(\omega_1 t + \phi) - (\omega_2 + \theta)] \quad (5)$$

The output E_o is the sum of equations (4) and (5) or $E_o = E_x + E_y$:

$$E_o = A_y \text{Cos } \omega_1 t \, A_x \text{Cos } (\omega_1 t + \phi) + B_y [\text{Cos } (\omega_1 + \omega_2)t + \text{Cos } (\omega_1 - \omega_2)t] + B_x [\text{Cos}[(\omega_1 + \omega_2)t + (\phi + \theta)] + \text{Cos}[(\omega_1 - \omega_2) + (\phi - \theta)]] \quad (6)$$

By letting

$A_x = A_y = 0$ (case of mixers and signals being perfectly balanced with no harmonics)

$B_x = B_y$

and

$\theta = \phi = 90°$

$E_o = B_x [\text{Cos}(\omega_1 + \omega_2)t + \text{Cos}(\omega_1 - \omega_2)t + \text{Cos}(\omega_1 + \omega_2)t - \text{Cos}(\omega_1 + \omega_2)t]$

$B = 2B_x$

Simplifying

$$E_o = B \text{ Cos}(\omega_1 - \omega_2)t \quad (8)$$

Equation (8) shows that the output of the single sideband mixer is a difference frequency when the phase shifts are both 90 degrees leading.

Figure 3 is a block diagram representing the R-390A receiver and the calibration technique.

If the incoming signal f_1 is in the frequency range of 0.5 to 8 MHz, the first local oscillator (LO_1) is switched on and f_1 is up converted in mixer 1 to 17.5 to 25 MHz and fed through IF_1 to mixer 2. If f_1 is above 8 MHz, it is switched directly into mixer 2 where it is mixed with the second local oscillator frequency, ranging from 11 to 34 MHz, and is down converted to 2 to 3 MHz. From the second mixer, the signal flows through the second IF into mixer 3 where it is combined with the third local oscillator frequency of 2.455 to 3.455 MHz to yield a third IF frequency of 455 kHz.

Taking specific examples:

a.			b.		
f_1	=	6.720 MHz	f_1	=	6.720 MHz
LO_1	=	17.000 MHz	LO_1	=	17.072 MHz
IF_1	=	23.720 MHz	IF_1	=	23.792 MHz
LO_2	=	26.000 MHz	LO_2	=	26.006 MHz
IF_2	=	2.280 MHz	IF_2	=	2.214 MHz
LO_3	=	2.735 MHz	LO_3	=	2.669 MHz
IF_3	=	0.455 MHz	IF_3	=	0.455 MHz

From the equation:

$$f_{input} = \left[f_{LO_2} - (f_{LO_3} - f_{IF_3}) \right] - f_{LO_3}$$

a. $f_i = 26.00 - (2.735 - 0.455) - 17.00$

$f_i = (26.00 - 2.28) - 17.00$

$f_i = 23.72 - 17.00$

$f_i = 6.72$ MHz

b. $f_i = 26.006 - (2.669 - 0.455) - 17.072$

$f_i = 26.006 - 2.214 - 17.072$

$f_i = 23.792 - 17.072$

$f_i = 6.720$ MHz

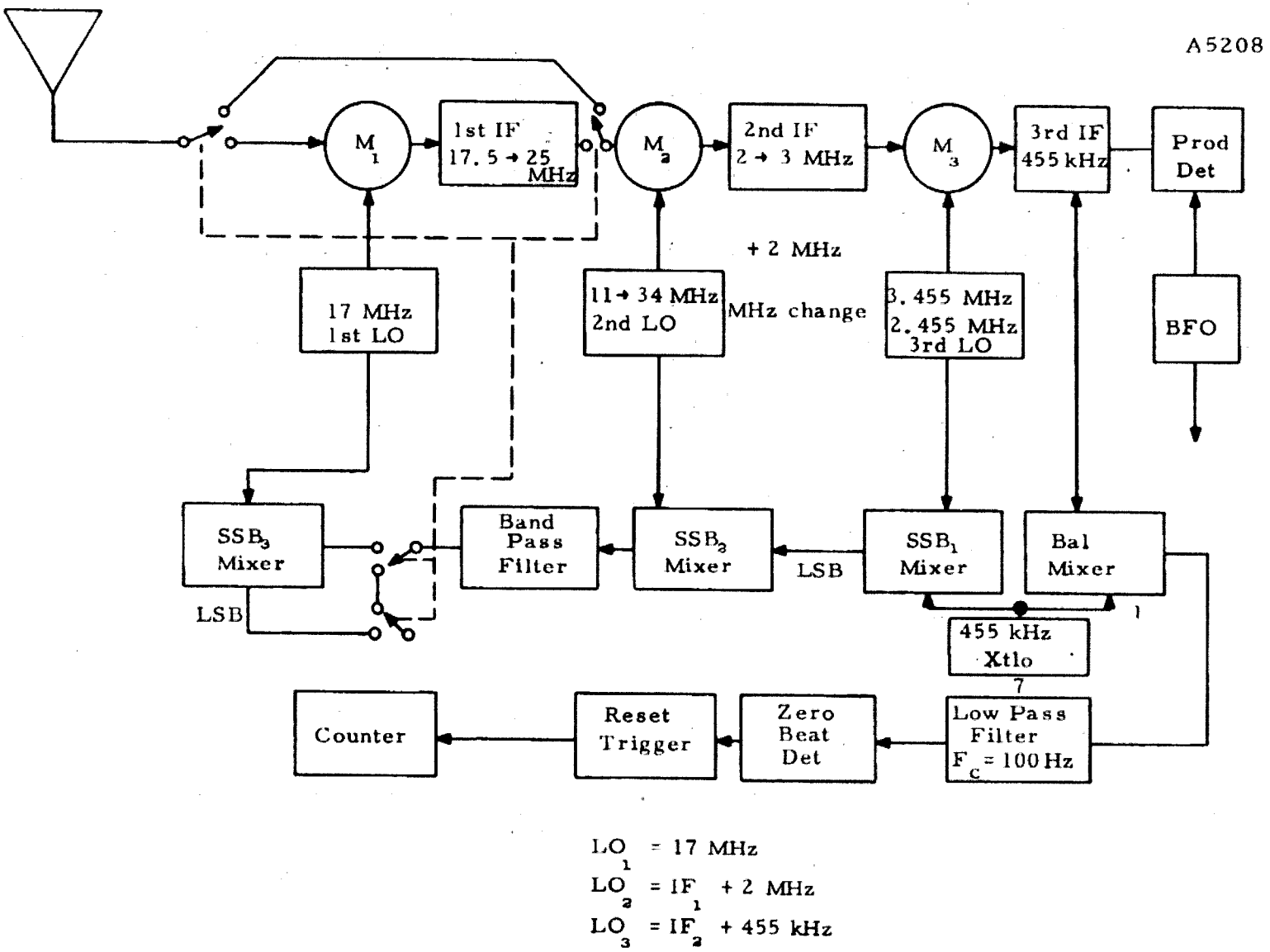

FIGURE 3 SSB Calibration Method Block Diagram (U)

The examples illustrate that by correctly subtracting the local oscillators the input frequency can be obtained. They also illustrate the fact that the local oscillators do not have to be exactly on frequency to obtain a correct calibration figure. These examples were composed under the premise that the third IF was tuned to exactly 455 kHz. This is not always true; in fact, it is seldom true. Assuming that the third IF is tuned to 457 kHz under the present premise the calibration figure is off by 2 kHz. To remedy this situation, the 455 kHz crystal oscillator is made tunable over a reasonable deviation from 455 kHz to allow for the difference in tuning of the receiver.

To insure that the 455 kHz variable oscillator is at the same frequency as the third IF, a zero beat detector is used. To detect a zero beat, the two signals are fed into a balanced mixer. The output of the mixer is fed through a low pass filter and into a saturating amplifier. The output of the amplifier is connected to a set of earphones completing the aural zero beat detector

Once a zero beat has been detected the LO's are subtracted by using the single sideband technique in the manner described by equation (10).

$$\text{input} = f_{LO_2} - (f_{LO_3} - f_{IF_3}) - f_{LO_1} \qquad (10)$$

The output of the last SSB mixer is fed into a counter and the input frequency is displayed. There are two conditions that make the use of an SSB configuration difficult. The first is that the two input signals must be exactly the same power level in order to completely eliminate the unwanted sideband term. Second, the harmonic content of the input should be very low due to the characteristics of the counter as the counter will count the fundamental frequency correctly only if the sum total of all the harmonics is less than the fundamental.

Both the third local oscillator and the 455 kHz oscillator are low in harmonic content and the power level of LO_3 varies little over the frequency range (2.455 MHz to 3.455 MHz) resulting in a lower sideband output in which the carrier is down about 70 dB. The output of SSB_1 mixer (Figure 3) is passed through a bandpass filter to further reduce the harmonics and then through an amplifier to increase the signal level.

Local oscillator 2 was designed as a harmonic oscillator in order to reduce the number of crystals required. The undesired modulation

products which occur due to the presence of the harmonics cannot be eliminated by filtering.

The result of using this method with the R-390A is that there is enough harmonic distortion in the output to cause a wrong count on the counter. This, coupled with the high cost of implementation, indicated the desirability of an alternate method of frequency subtraction.

3. FREQUENCY SUBTRACTION BY DIGITAL TECHNIQUE

The alternate method of performing the subtractions described by equation (10) utilizes a pulse elimination technique. Its operation is described below. There are two input pulse trains derived from the two frequencies to be subtracted. The pulse repetition frequency of one input must always be greater than the pulse repetition frequency of the second input. Every pulse of the faster pulse train is made available to the output through an inhibit gate. The gate is normally open and the pulses are allowed to reach the output. Whenever a pulse from the slower pulse train occurs, it closes the gate and prevents the faster pulse from reaching the output. When the pulses on the output are counted over a one-second interval, the resulting number is equal to the difference between the two pulse repetition frequencies.

This scheme lends itself readily to digital techniques eliminating the necessity of using expensive balanced modulators and wide bandwidth phase shifters. Due to the high frequency (30 MHz) it was found necessary to divide most of the input frequencies by 10 to be able to use state-of-the-art digital integrated circuits. This modifies the equation of the process:

$$\frac{f_{input}}{10} = \left[\frac{LO_2}{10} - \left(\frac{LO_3 - IF_3}{10} \right) \right] - \frac{LO_1}{10} \qquad (11)$$

Figure 4 is a block diagram of the calibrator using the digital method. The receiver and the frequency readout unit operate in exactly the same manner as in the SSB mode except that the subtraction is now performed digitally and frequency dividers are required. The previous example of pulse subtraction still applies. Since several advantages were realized by the digital technique, a prototype frequency readout model was developed and interfaced with

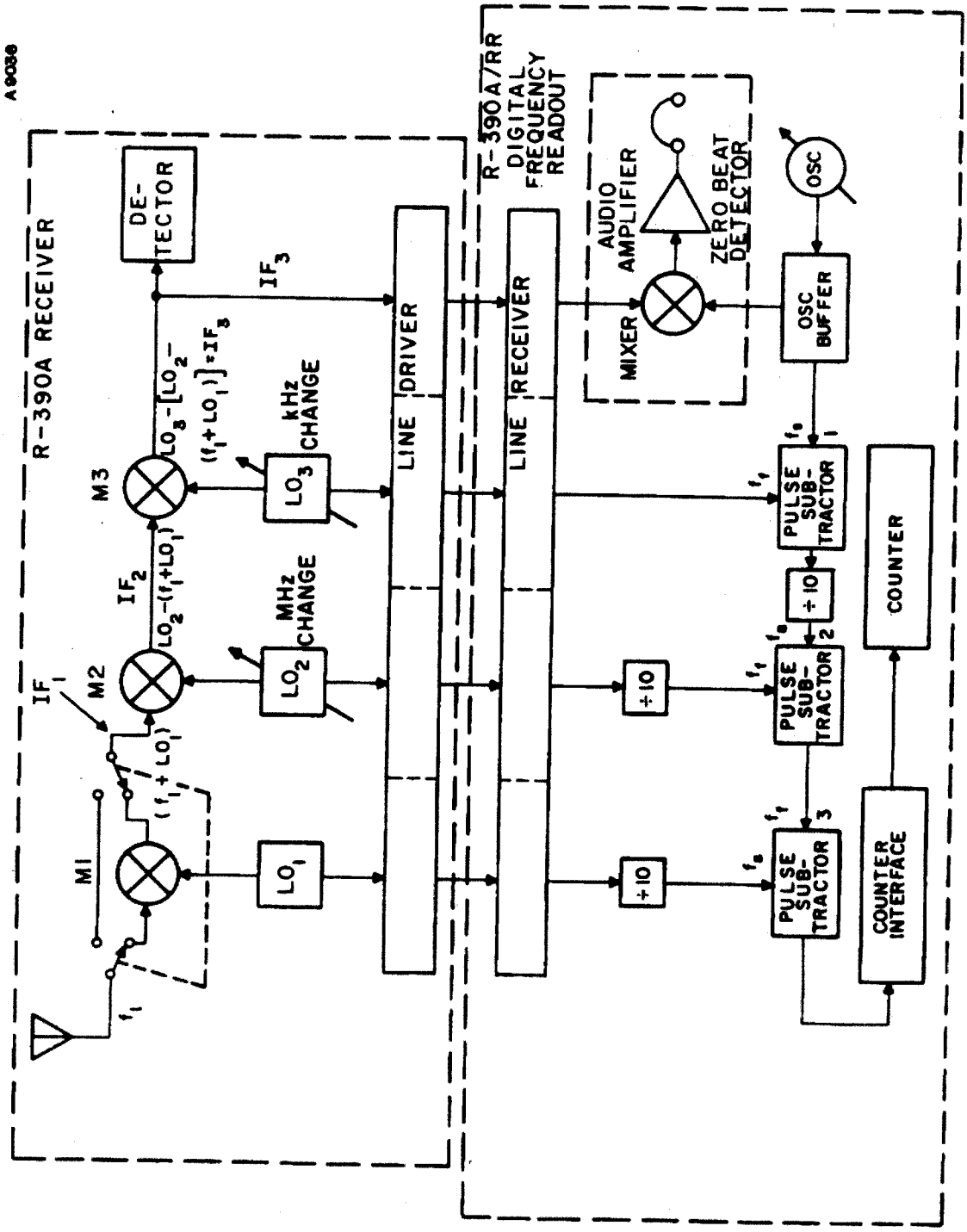

FIGURE 4 Block Diagram of the Digital Frequency Readout Unit and the R-390A Receiver (U)

an R-390A receiver. The heart of this technique is the pulse subtractor described in detail in a later section. In general, the equipment developed to realize the readout unit consists of interfacing circuits, frequency subtractors, a beat oscillator, and a Hewlett Packard frequency counter. Photographs of front and rear views of the R-390A Receiver/Digital Frequency Readout Unit are shown in Figures 5 and 6, respectively.

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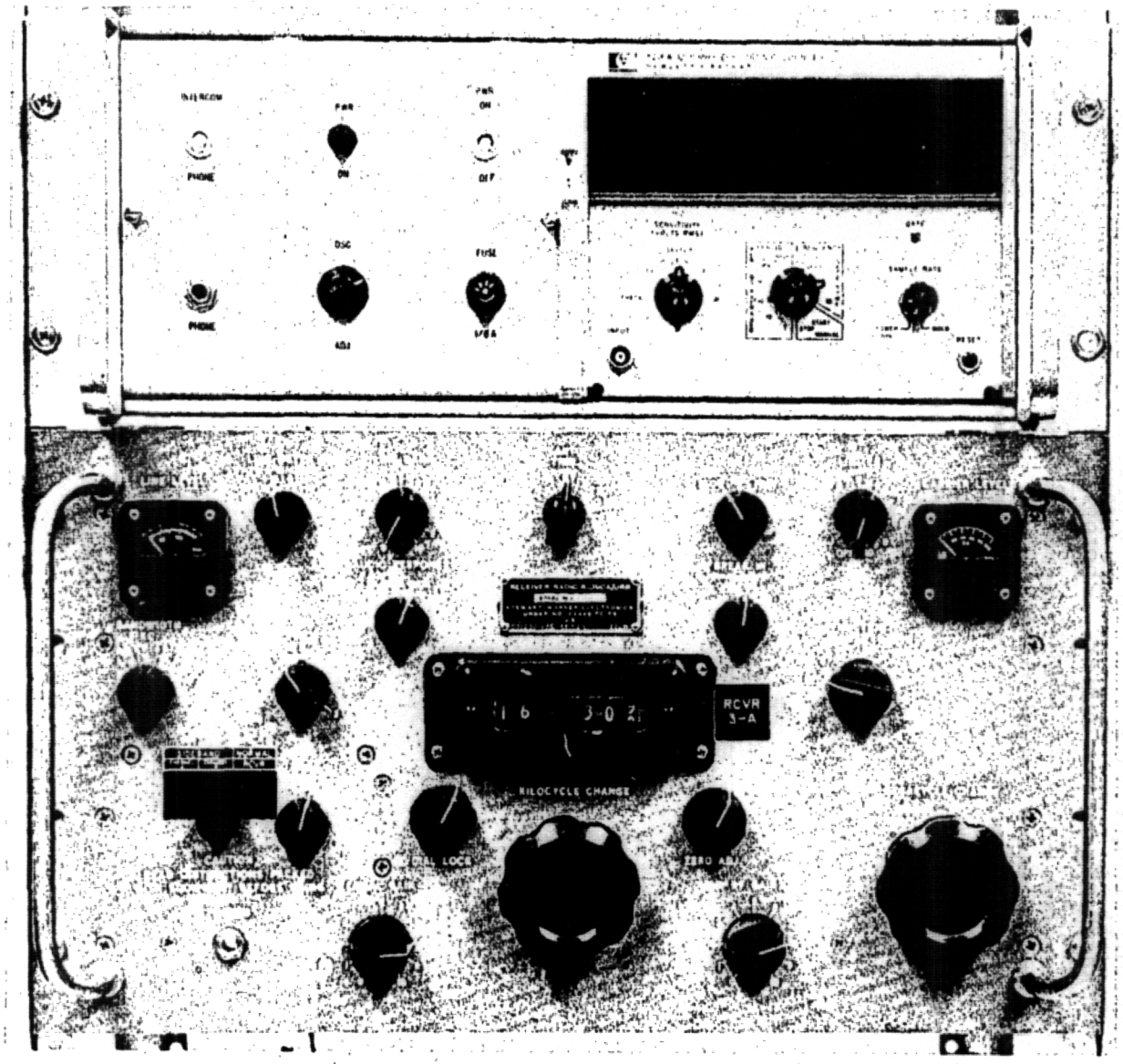

FIGURE 5 Front View of R-390A Receiver--Digital Frequency Readout Unit (U)

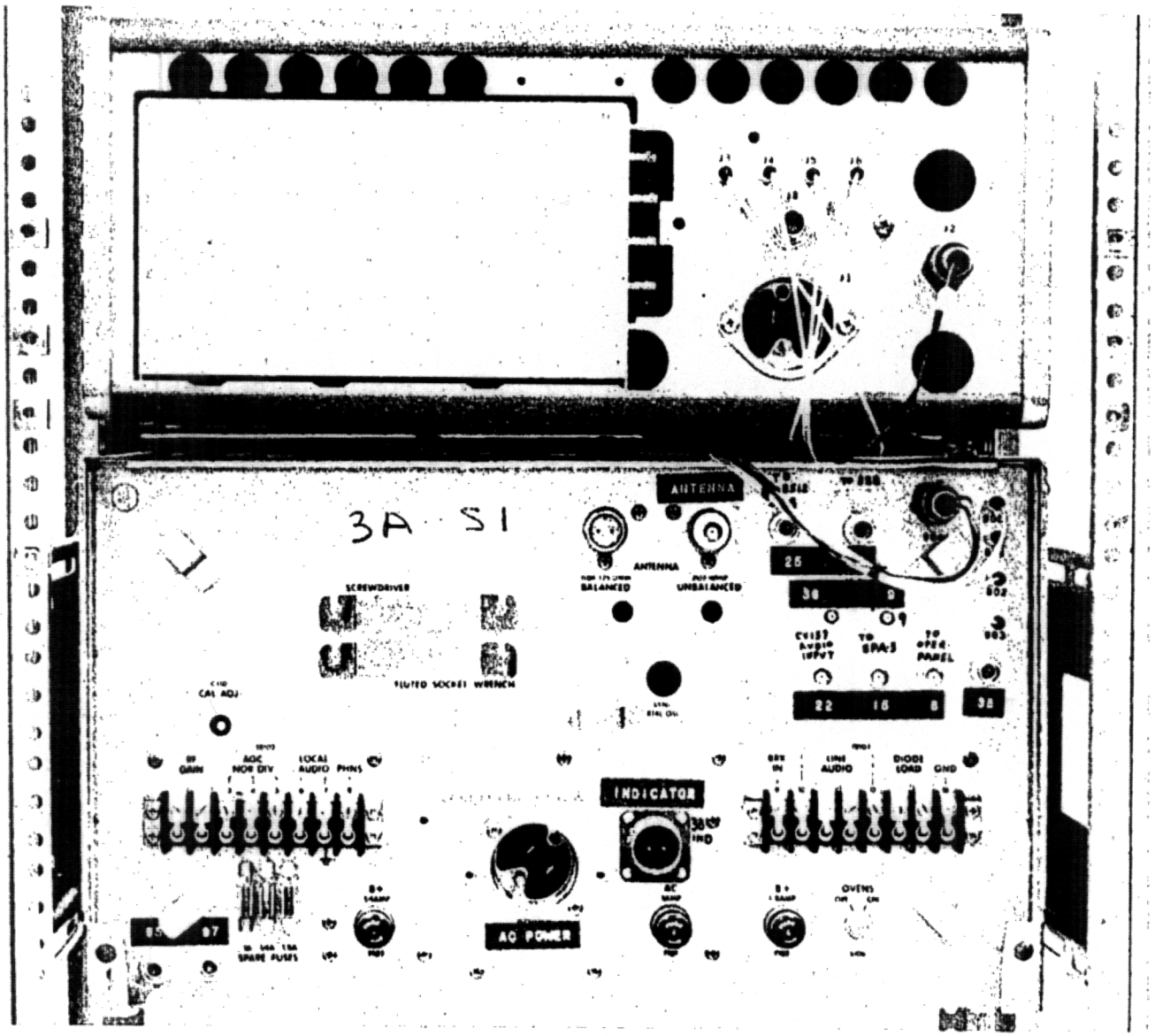

FIGURE 6 Rear View of R-390A Receiver--Digital Frequency Readout Unit (U)

SECTION III

THEORY OF OPERATION

1. DESCRIPTION OF BLOCK DIAGRAM

The block diagram of the R-390A receiver and the frequency readout unit is shown in Figure 4. The local oscillator (LO) and IF_3 signals are fed to the line drivers where buffering and amplification are performed. From the line drivers the signals are passed to the line receivers in the frequency readout unit. The reason for having line drivers and receivers is to reduce impedance mismatches due to long cables and connectors, to provide good isolation between the receiver circuitry and logic elements in the readout unit, and to provide sufficient drive for the logic circuitry.

The IF_3 and zero beat oscillator signals are fed to a mixer producing a low frequency audio signal which is amplified and brought out to a front panel phone jack. The oscillator frequency is also fed to the first pulse subtractor (PS 1) where it is subtracted from LO_3 frequency. The difference frequency ($f_f - f_s$) is divided by 10 and applied to PS 2 as the slow pulse train f_s. The $LO_2/10$ frequency is the f_f input to PS 2. The third subtractor performs the function of subtracting f_{10} from the output frequency of the second PS. The output from the last PS is equal to the input frequency of the receiver and is fed to the counter through the counter interface.

Since the LO and IF frequencies are divided by 10 in the logic circuits, the reading displayed by the counter will be 1/10 of the actual frequency.

2. LINE DRIVER (Figure 7)

The line drivers function as buffers between receiver circuitry and the calibrator. A total of four drivers are arranged in a single metal case which is divided into four separate compartments to provide individual shielding for the drivers reducing cross modulation. Loading of the local oscillators is kept to a minimum by mounting the line drivers in the receiver.

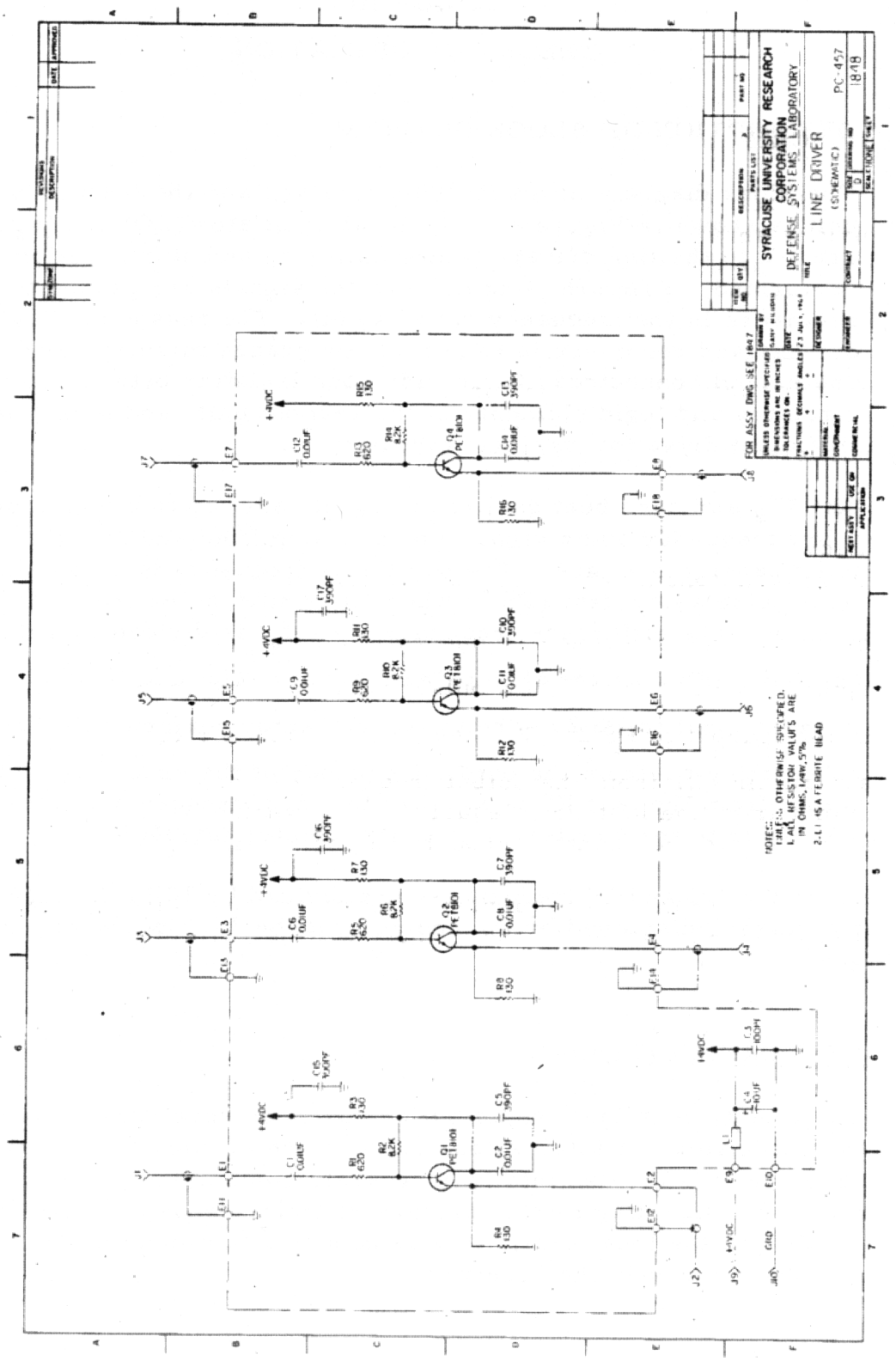

FIGURE 7 Line Driver (U)

The line driver is a modified emitter follower. A collector-to-base feedback resistor has been added to the general emitter follower configuration to improve dc stability.

3. LINE RECEIVER (Figure 8)

The line receiver is located in the frequency readout assembly. A grounded base input stage provides low input impedance correctly terminating the input line as well as isolation from the output. The grounded base amplifier drives an emitter follower. A clamping circuit on the output of the emitter follower essentially doubles the signal level by adding a dc component that is approximately equal to the peak value of the signal.

4. DIVIDE-BY-10 LOGIC

The function of the divide-by-10 logic is to divide the input frequency by 10, because the subtraction logic can operate with frequencies only up to approximately 5 MHz. Since the highest frequency input, contributed by LO_2, is about 34 MHz, the division must be performed before the pulse subtraction technique will work. The result of division by 10 is that the input equation becomes:

$$\frac{f_{input}}{10} = \left[\frac{f_{LO_2}}{10} - \left(\frac{f_{LO_s} - f_{IF_s}}{10} \right) \right] - \frac{f_{LO_1}}{10}$$

The effect of dividing by 10 is to reduce the accuracy to $\pm$ 10 Hz in 10^8 Hz for a count of one second.

Figure 9a is a simplified diagram of the divide-by-10 logic and Figure 9b is the truth table of the binary element. The divide-by-10 process is described by the truth table of Figure 9c. The output waveform is nonsymmetrical with a 20 per cent duty cycle.

5. PULSE SUBTRACTOR

The pulse subtractor provides a low cost, real time method of deriving the difference between two input frequencies. Coupled with a counter and a one-second time gate, the pulse subtractor will yield the difference frequency of two input signals.

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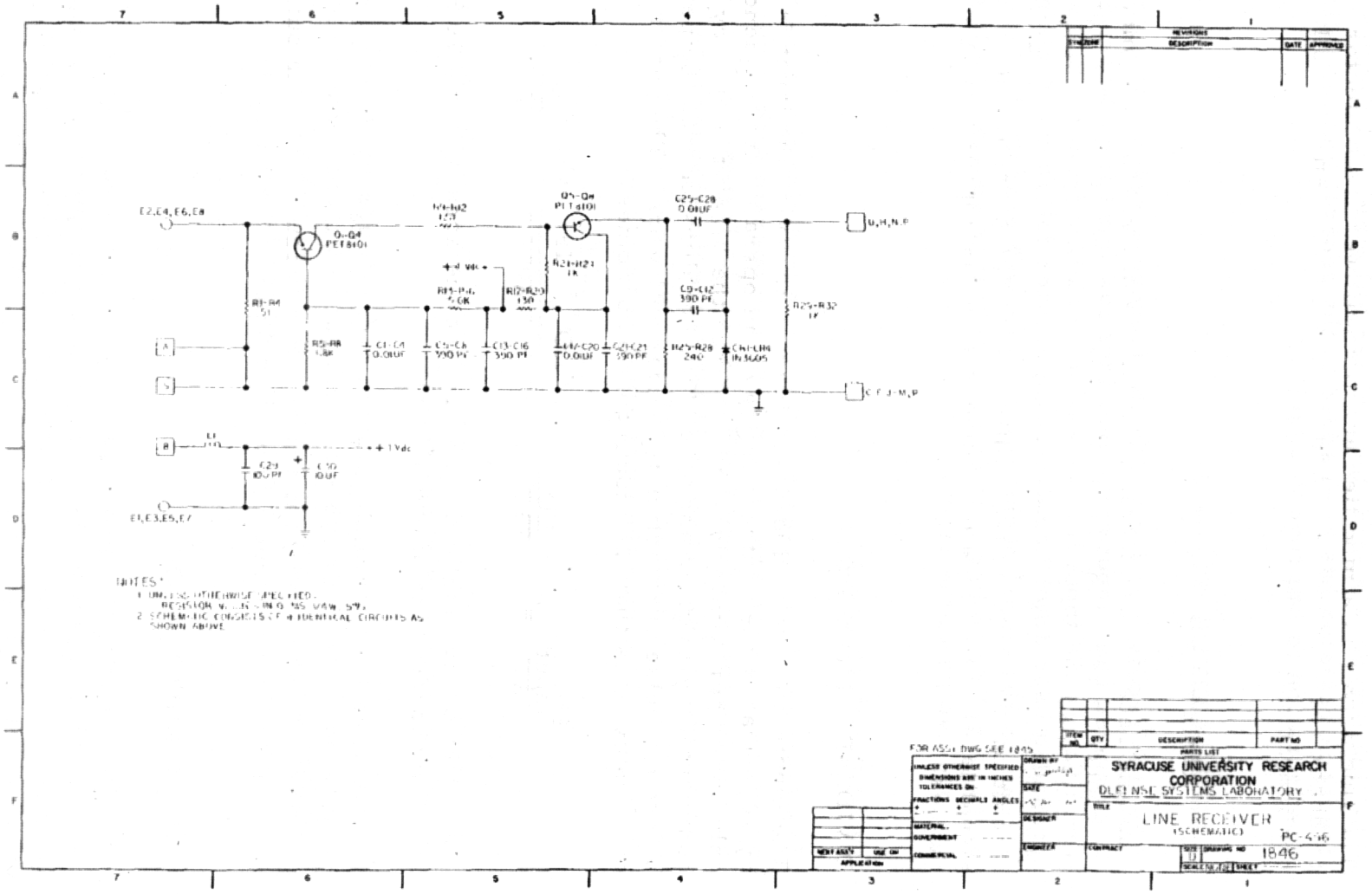

FIGURE 8 Line Receiver (U)

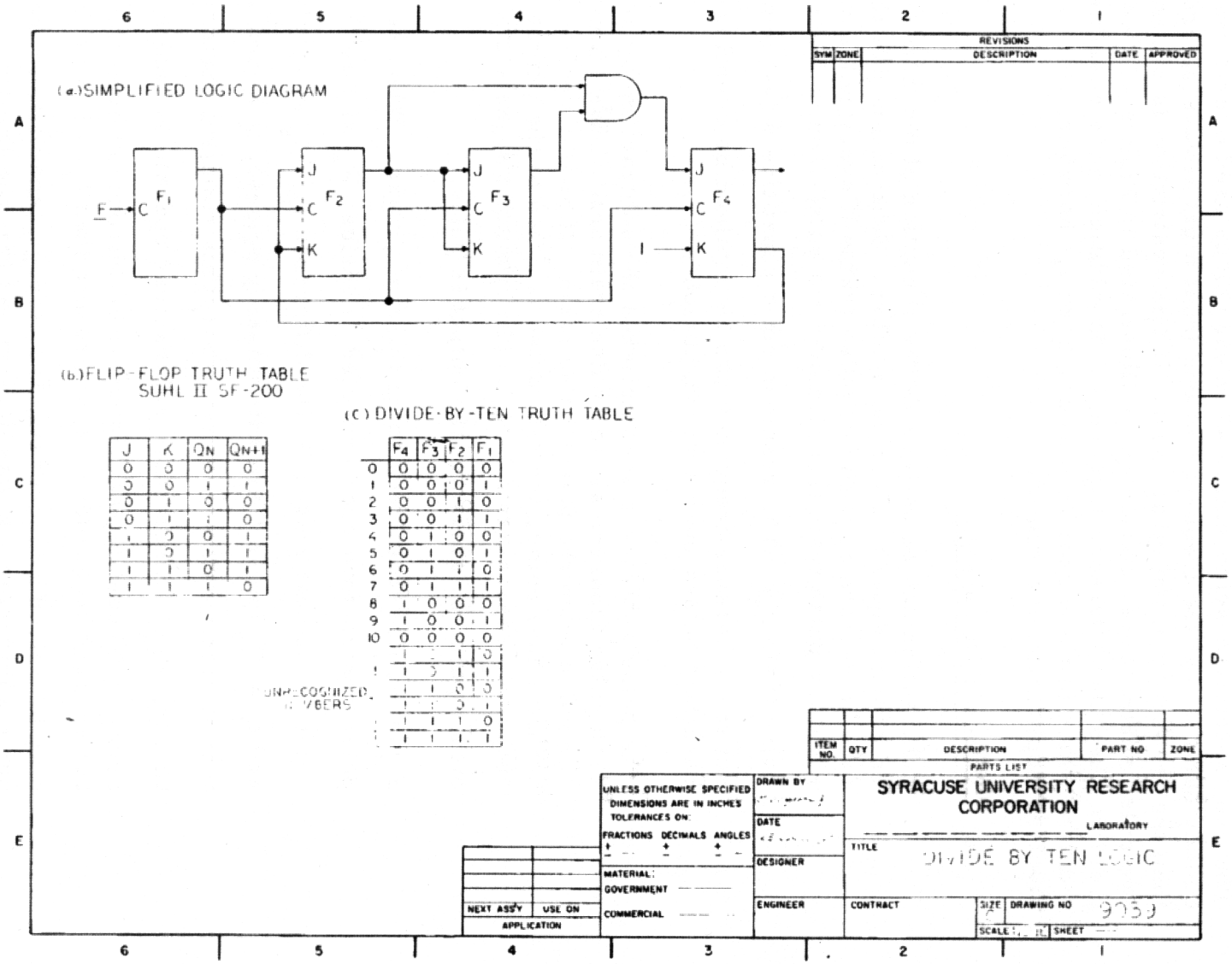

FIGURE 9 Divide-by-10 Logic (U)

The one restriction which exists when the unit is used over a frequency band is that the frequency of one input must always be greater than the frequency of the other input. If this restriction is undesirable, two pulse subtractors, connected as illustrated in Figure 10, will yield an absolute difference frequency. In addition, it is possible to indicate which is the higher frequency, f_1 or f_2; however, this involves duplication of circuits.

a. General Discussion

Subtraction can be defined as the reduction of one number by an amount equal to a second number. Subtraction can therefore be performed with two pulse trains if every pulse from a slower pulse train (f_s) eliminates a pulse from a faster pulse train (f_f). The result is not a repetitive waveform, but the difference frequency can be obtained by counting the resultant pulses over a known period.

The pulse subtractor accomplishes the subtraction by storing each pulse from the slower pulse train until it has eliminated one pulse from the faster pulse train. If no slow pulse occurs before a fast pulse, the fast pulse is gated to the output. The output F_o represents $f_f - f_s$. The two input signals can be either pulse or sinusoid; the output is pulse.

F_o is a pulse train with some missing pulses. When several pulse subtractors are connected in series, F_o will be the input to the next stage. If the difference $f_f - f_s$ is small, and $f_f = F_o$ (pulse train with missing pulses), it is possible that at some instant of time $f_s > f_f$ thus violating the restriction ($f_f > f_s$). Since pulse subtractors operate in real time, error in frequency reading would be introduced even though the average frequency of f_f is greater than f_s. The problem may be solved by increasing the storage capability in the pulse subtractor. It was determined that the Digital Frequency Readout Unit would require three pulse subtractors connected in series. The first two pulse subtractors require

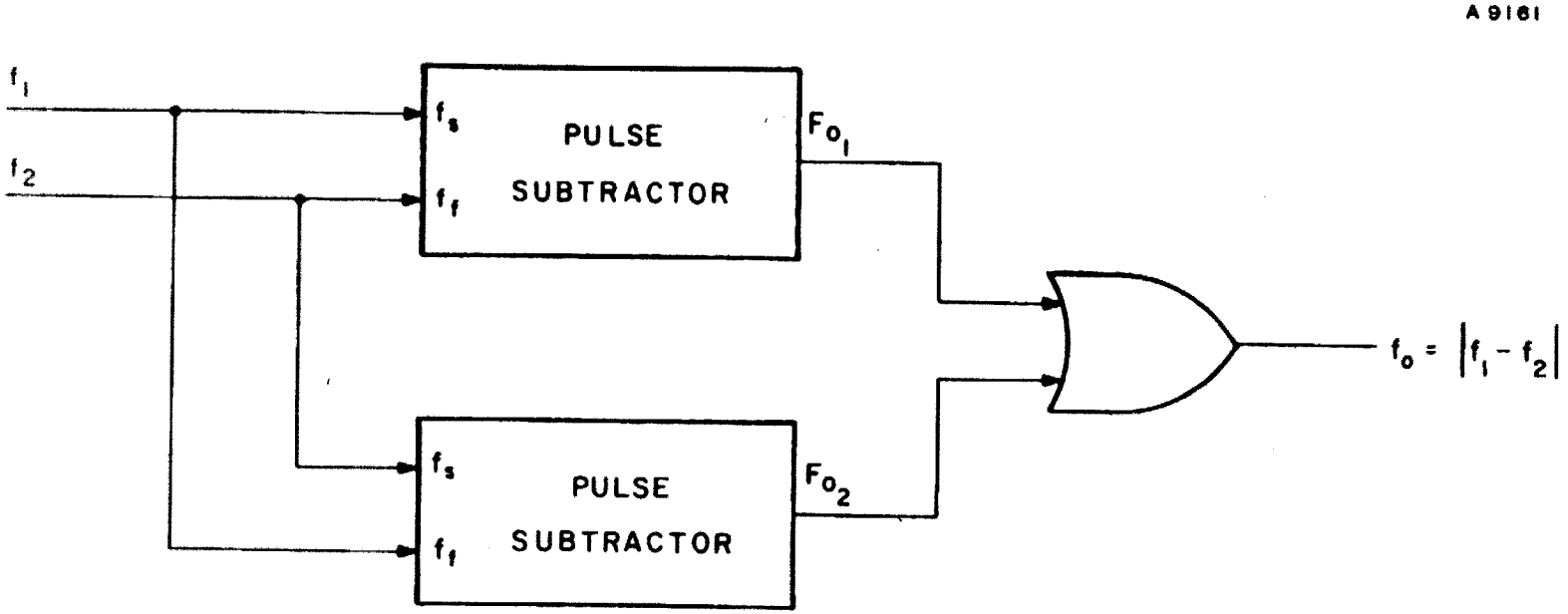

FIGURE 10 Absolute Value of Difference Frequency Block Diagram (U)

one storage element, but the third stage requires two for proper operation. Since the difference between the two circuits are significant they will be discussed separately.

b. Logic Theory, One Memory Element

There are five basic blocks which require only 22 TTL gates as active elements.

Referring to the block diagram (Figure 11), f_f is the higher frequency input. This input is shaped and fed into the sync generator which produces three consecutive pulses for each f_f input pulse. The three pulses respectively reset the inhibit, sample the memory, and provide a pulse for the output.

f_s is the lower frequency input; it is shaped and stored in the memory. The transfer gate's function is to transfer information from the memory to the inhibit at the correct time as determined by the sync generator. The inhibit closes the output gate and insures that there is no output pulse.

The sequence of operation would be as follows (see Figure 12): An f_s pulse is followed by an f_f pulse. The f_s pulse is stored in the memory; the f_f pulse causes the sync generator to produce three pulses. Pulse one resets the inhibit which opens the output gate. Pulse two opens the transfer gate, which is normally closed, and transfers the information stored in the memory to the inhibit. When the information transfer has been completed, the memory is reset. The inhibit closes the output gate. Pulse three is not passed through the output gate, thus, there is no output.

Considering the other possible sequence in which an f_s pulse follows an f_f pulse, the f_f pulse causes the sync generator to produce three pulses. Pulse one resets the inhibit and opens the output gate. Pulse two opens the transfer gate, but there is no information in the memory to be transferred and the inhibit is not set. Since the inhibit was not

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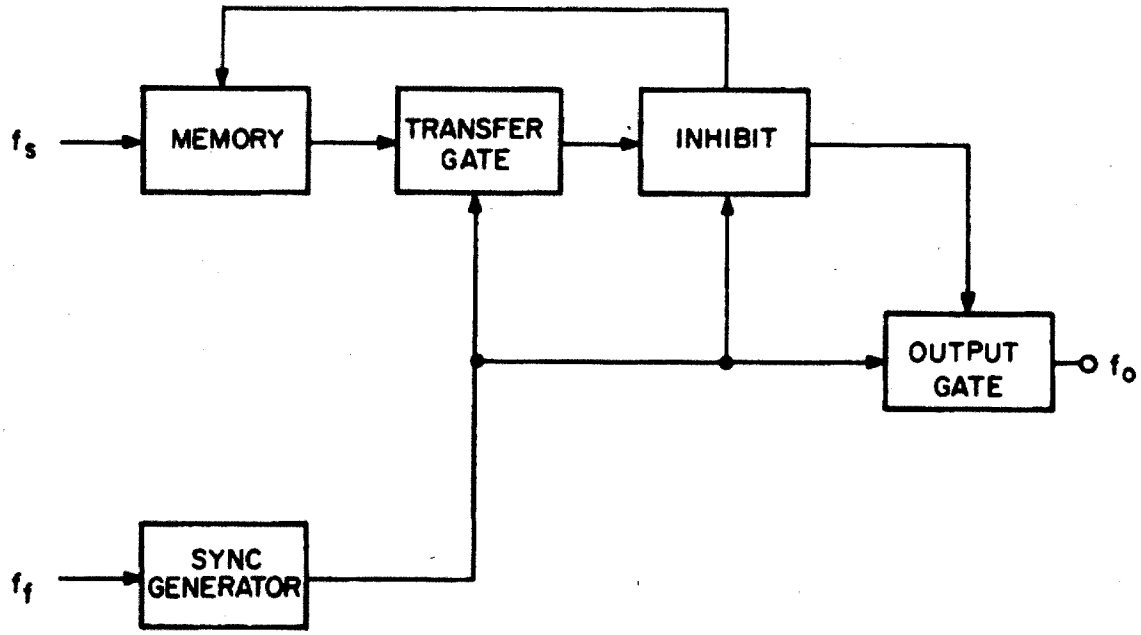

FIGURE 11 Pulse Subtractor Block Diagram (U)

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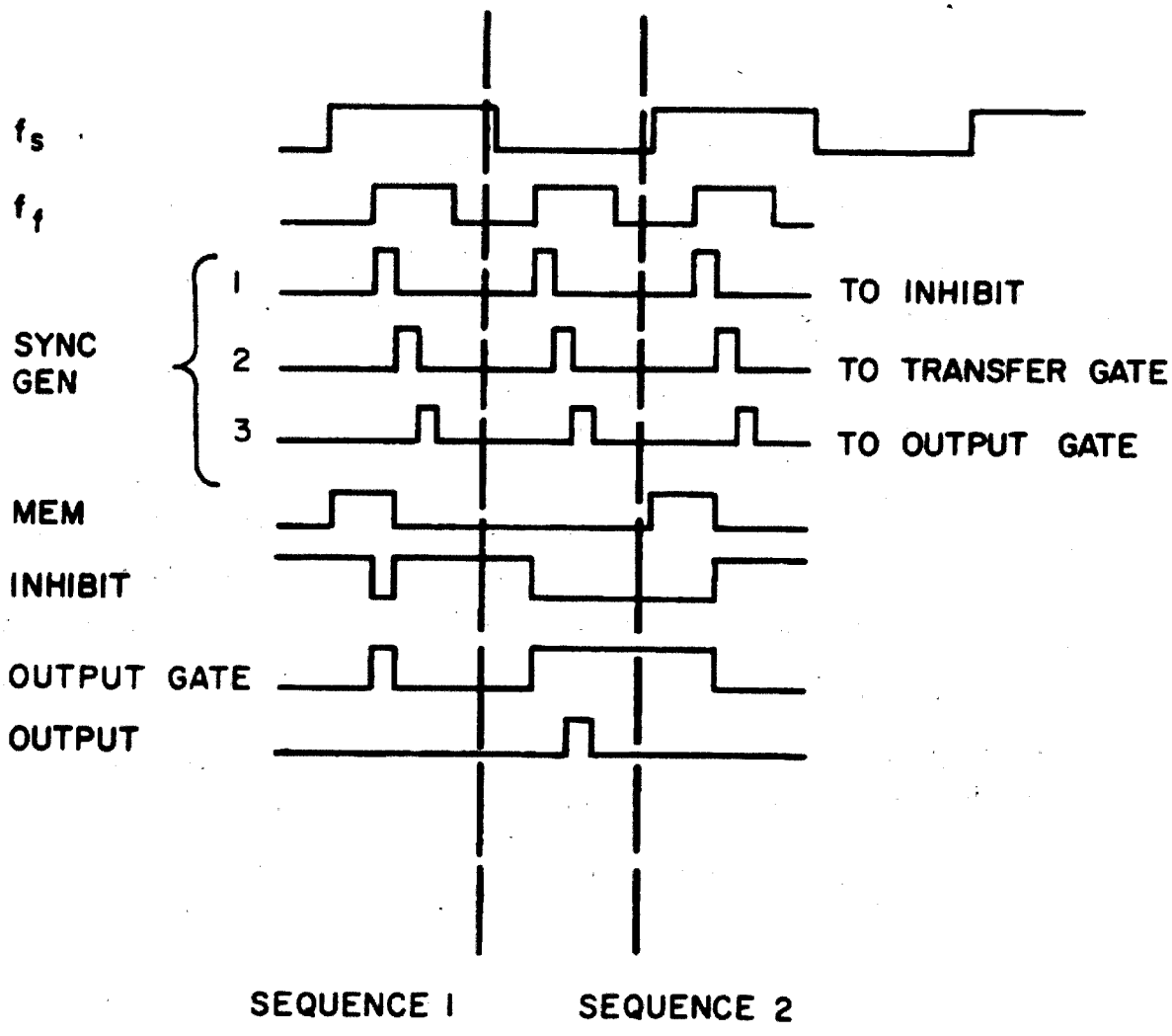

FIGURE 12 Time Sequence Diagram (U)

set, the memory is not reset. Pulse three is passed through the output gate to the output. If f_f and f_s occur at precisely the same time the logic treats the occurence in the same manner as when an f_s pulse follows an f_f pulse (sequence 2, Figure 12). The logic eliminates the chance of a race.

c. Logic Theory, Two Memory Elements

The third pulse subtractor contains two memory elements and additional logic to control the timing. The theory of operation is similar to the first two pulse subtractors but the modifications require further discussion.

The pulse subtractor consists of eight function blocks: a sync generator, two memory elements, two transfer gates, an inhibit gate, and an output gate. A block diagram is shown in Figure 13.

The input signals f_s and f_f are the lower and higher frequency inputs, respectively. f_f pulses are fed to the sync generator which develops three consecutive pulses for each f_f input pulse. The first pulse from the sync generator is fed to Transfer Gate I and allows the transfer of information from Memory I to Memory II. A second pulse goes to the inhibit gate; and, if an inhibit pulse from Memory II is not present, an output pulse is generated. Finally, the third pulse from the sync generator is used to reset Memory II. The low frequency pulse (f_s) is fed to Memory I and Transfer Gate II; f_s is propagated through this transfer gate to Memory II only if Memory I was set before the occurence of the next f_s (that is, two consecutive f_s pulses occur before an f_f pulse). The transfer gate also generates an inhibit function for the reset pulse of Memory I, thus preventing loss of information.

Memory II could be set in two ways. If only one f_s pulse occurs in sequence, it is stored in Memory I and when the f_f arrives, the information is transferred to Memory II.

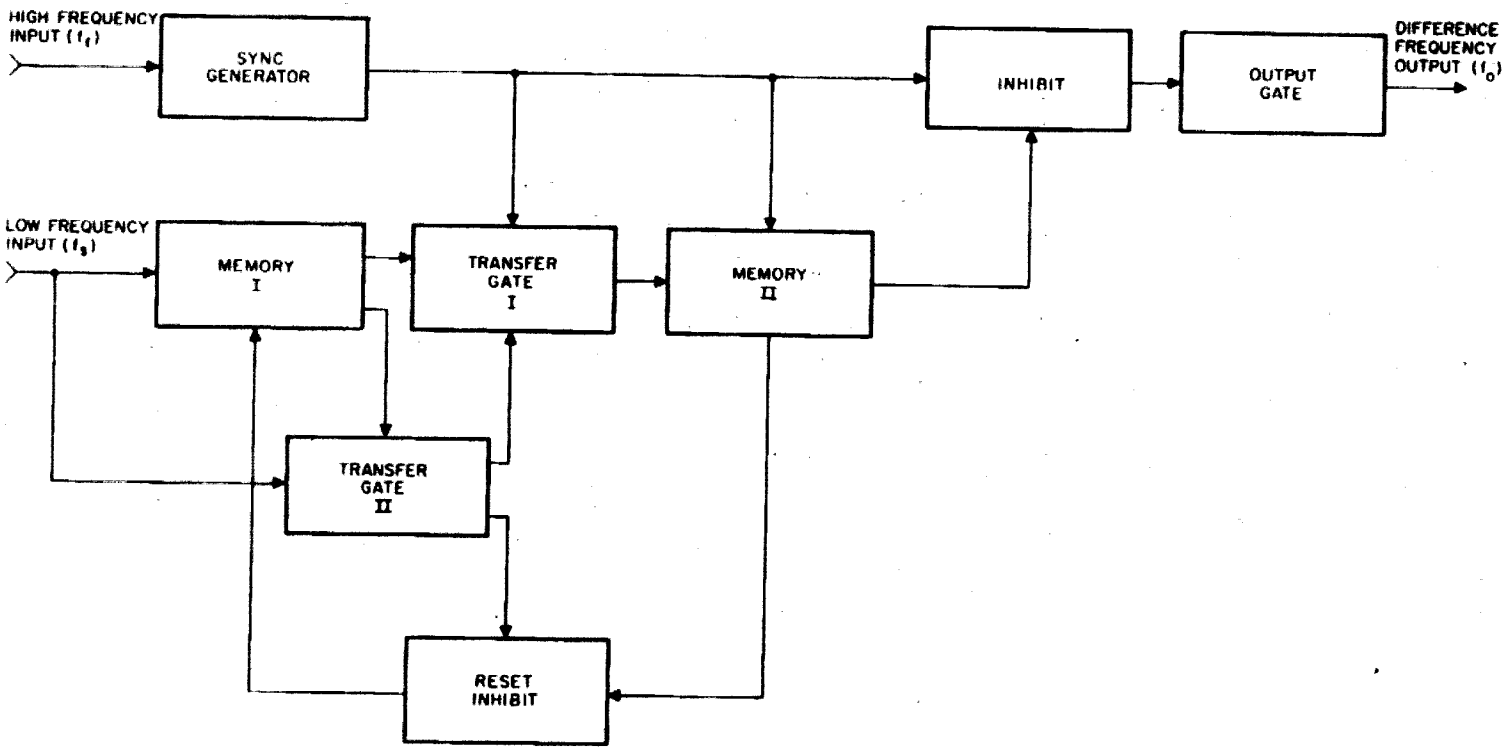

FIGURE 13 Block Diagram of the Pulse Subtractor (Mod I) (U)

An inhibit function is generated which cancels the f_f pulse and a reset pulse is propagated to Memory I. Memory II is reset immediately after the occurence of f_f.

On the other hand, if two f_s pulses occur in sequence, the first is stored in Memory I and the second in Memory II through Transfer Gates I and II. To prevent resetting of Memory I under this condition (thus loss of information) a reset inhibit function is generated which blocks the reset pulse.

By using the above scheme none of the f_s pulses are lost and the correct frequency is presented to the counter.

d. Detail Operation of the Pulse Subtractor

The only active element used in the pulse subtractor is a quad two input TTL gate. The use of this element in the fabrication of a monostable multivibrator (OSM), a basic building block, is described in detail in the following section. The second building block, a set-reset flip-flop, is a cross-coupled nand illustrated in Figure 14.

The following discussion applies to both types of pulse subtractors unless indicated otherwise. The schematics of the subtractors are shown in Figures 15 and 16.

(1) Input Shaping

The input signal is shaped by a single nand gate. The waveform can be of any repetitive shape with maximum peaks no greater than 5.5 volts and minimum peaks no less than 0.5 volts.

The output of the shaper is a pulse with rise and fall time in the order of 10 ns.

(2) Sync Generator

This logic function produces three successive pulses approximately 30 ns wide. The pulses are the result of three monostable circuits connected in series. As

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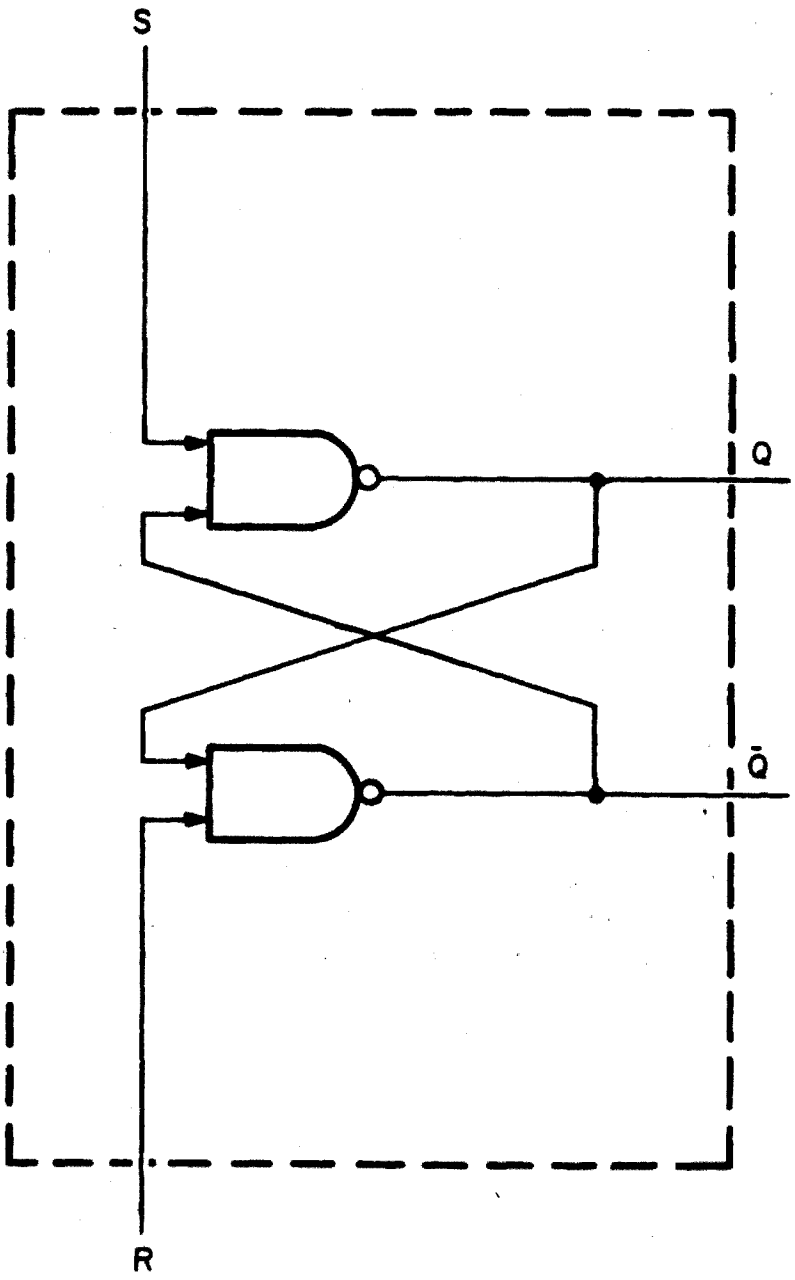

FIGURE 14 Set-Reset Flip-Flop (U)

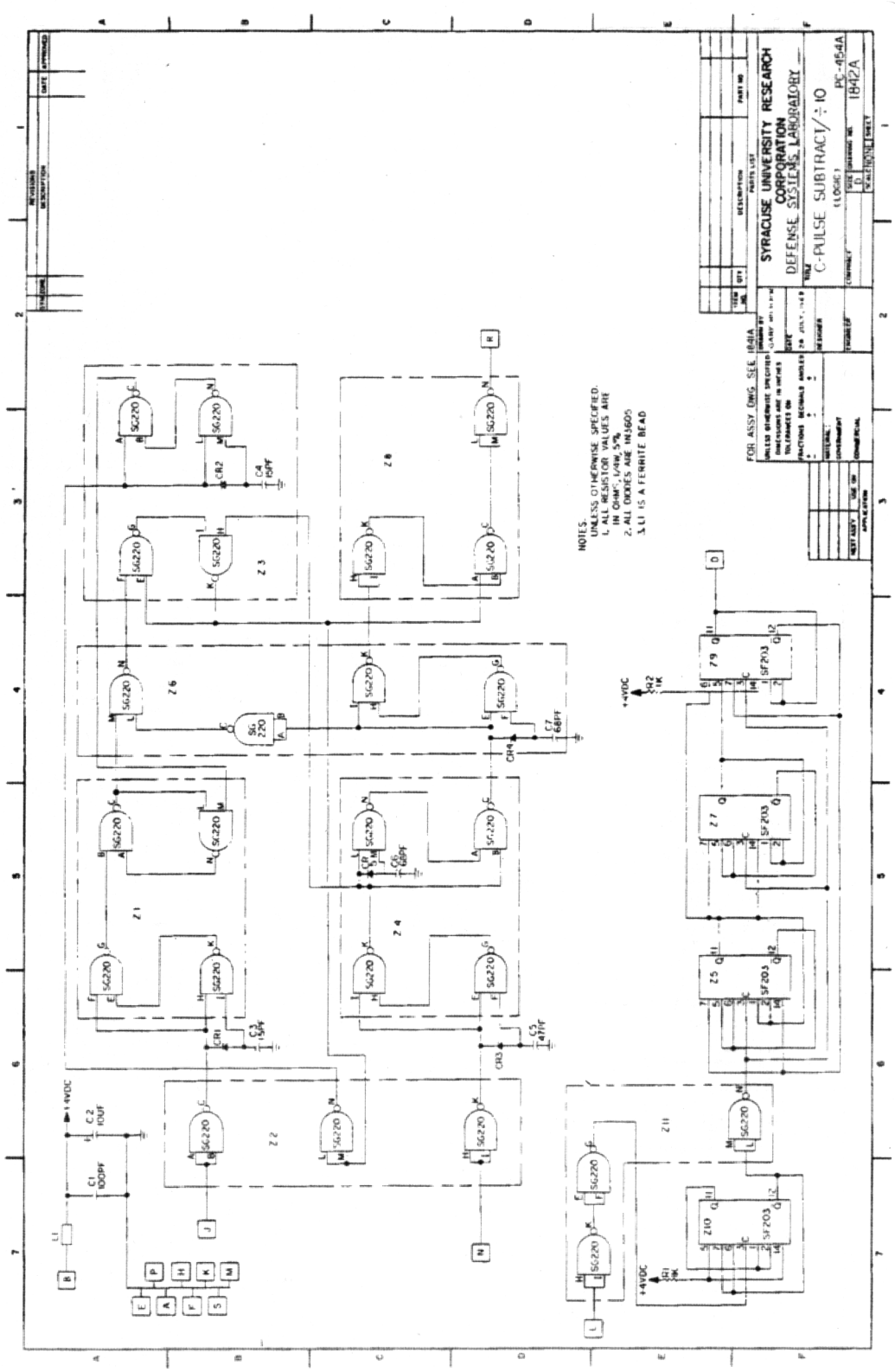

FIGURE 15 C-Pulse Subtract/Divide-by-10 Logic (U)

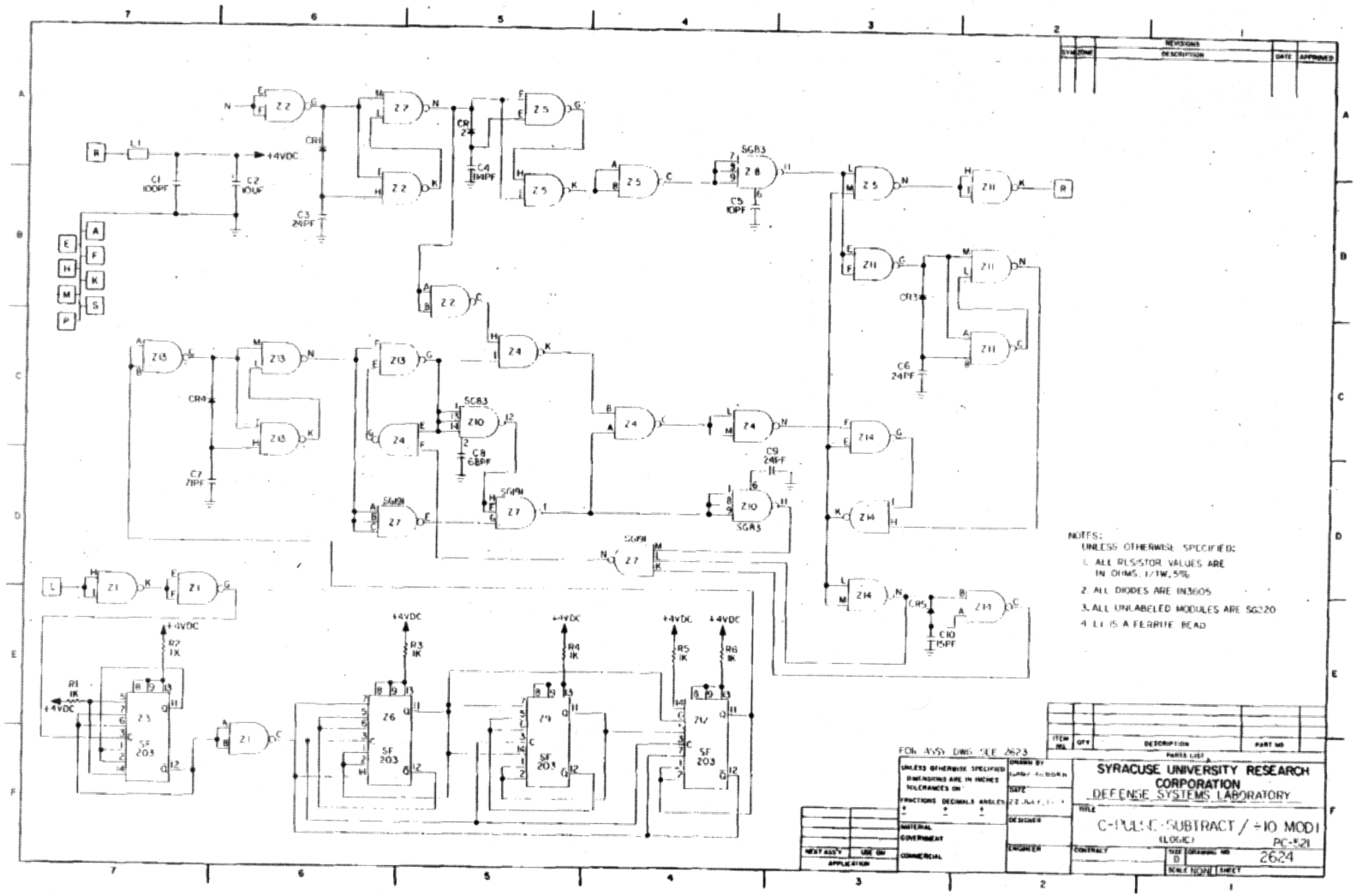

FIGURE 16 Pulse Subtractor Divide-by-10 Logic (U)

the output of a monostable is a negative pulse, a second monostable connected to the output of the first will produce a pulse when the first pulse returns to a plus level. A set of three pulses occurs for every f_f (fast frequency) pulse. This limits the fastest frequency to about 8 MHz.

(3) Memory

The memory stores an f_s (slow frequency) pulse until it is ready to be used. The input pulse is narrowed to a width of about 20 ns by a monostable unit. The narrow negative pulse sets the Q output of an R-S flip-flop to one. f_1 remains in a "1" state until the flip-flop receives a pulse from the inhibit block indicating that the stored information has been transferred. When the reset pulse is received, the Q output of f_1 is reset to zero and the memory is ready to accept new information.

(4) Transfer Gate

The transfer gate performs its gating function and may consist of one or more logic elements. Upon command from a sync generator or some other timing function, the information present at the input of the gate (a "0" or a "1") will be transferred to the output.

In the Memory I pulse subtractor information is transferred from memory to inhibit upon command from the second pulse of the sync generator.

In the case of the third pulse subtractor, where two storage elements are incorporated, command is given by the first pulse of the sync generator and a "1" or a "0" from Memory I is transferred to inhibit. The inhibit element functions as Memory II if consecutive f_s pulses occur.

(5) Transfer Gate II

If two consecutive f_s pulses occur, the first is stored in Memory I, but is not passed through the transfer

gate. Command to pass the pulse is generated by the Q output of Memory I only if the pulse arriving is the second consecutive f_s pulse. This is accomplished by delaying the Q output; the time delay is equal to or greater than the pulse width of f_s. Two outputs are provided by the transfer gate; one is used to "set" Memory II and the second is fed to the reset inhibit to prevent the resetting of Memory I.

(6) Inhibit

The inhibit, or Memory II (as referred to in the third pulse subtractor), consists of a flip-flop and a monostable element. This logic stores the second consecutive f_s pulse and inhibits the output gate whenever an f_s pulse occurs. It also produces a reset pulse for Memory I. When a "1" is transferred from Memory I or from Transfer Gate II, indicating that an f_s pulse has occurred, the $\overline{Q}$ output is forced to a "0" inhibiting the output gate and triggering a monostable element to provide a reset pulse for Memory I. The inhibit logic is reset by one of the sync generator pulses.

(7) Reset Inhibit

The reset inhibit consists of a time delay element and a three input NAND gate. This logic controls the resetting of Memory I and insures that only one memory element is reset with the occurence of an f_f pulse, thus preventing loss of information.

(8) Output Gate

The output gate provides for the actual subtraction process. Every time an f_f pulse occurs, the sync generator presents a pulse to the output gate. The pulse is created by the second or third monostable element in a chain of three. If there is no inhibit,

the pulse is gated to the output; if there is an inhibit, the pulse does not reach the output. The result is a pulse train representing $f_f - f_s$.

(9) Timing

Timing in the pulse subtractor is very important. By maintaining the proper pulse width ratios the pulse subtractor will have no race conditions and will subtract frequencies which are only a fraction of a cycle apart.

If, after every f_s pulse an f_f occurs, the timing sequence is similar in all three pulse subtractors (PS); however, if two consecutive f_s's arrive, as could be the case in the third PS, additional timing problems arise. The general case will be described first.

(10) Timing Sequence, Pulse Subtractors 1 and 2

Since each f_s pulse must inhibit an f_f pulse, each P_4 pulse must set the memory. The time needed to complete a full cycle of setting and resetting the memory determines the maximum slow frequency. The logic diagrams of both circuits are shown in Figures 15 and 16.

There are three possible combinations of pulses that are presented to the transfer gate. Relating to Figure 17:

(a) Point A -- P_2 occurs after the memory has been set

(b) Point B -- P_2 occurs before the memory has been set but is still coincident

(c) Point C -- P_2 occurs before the memory has been set and is not coincident *

---

* Point C is not considered a coincidence because the resulting pulse is too narrow to be propagated.

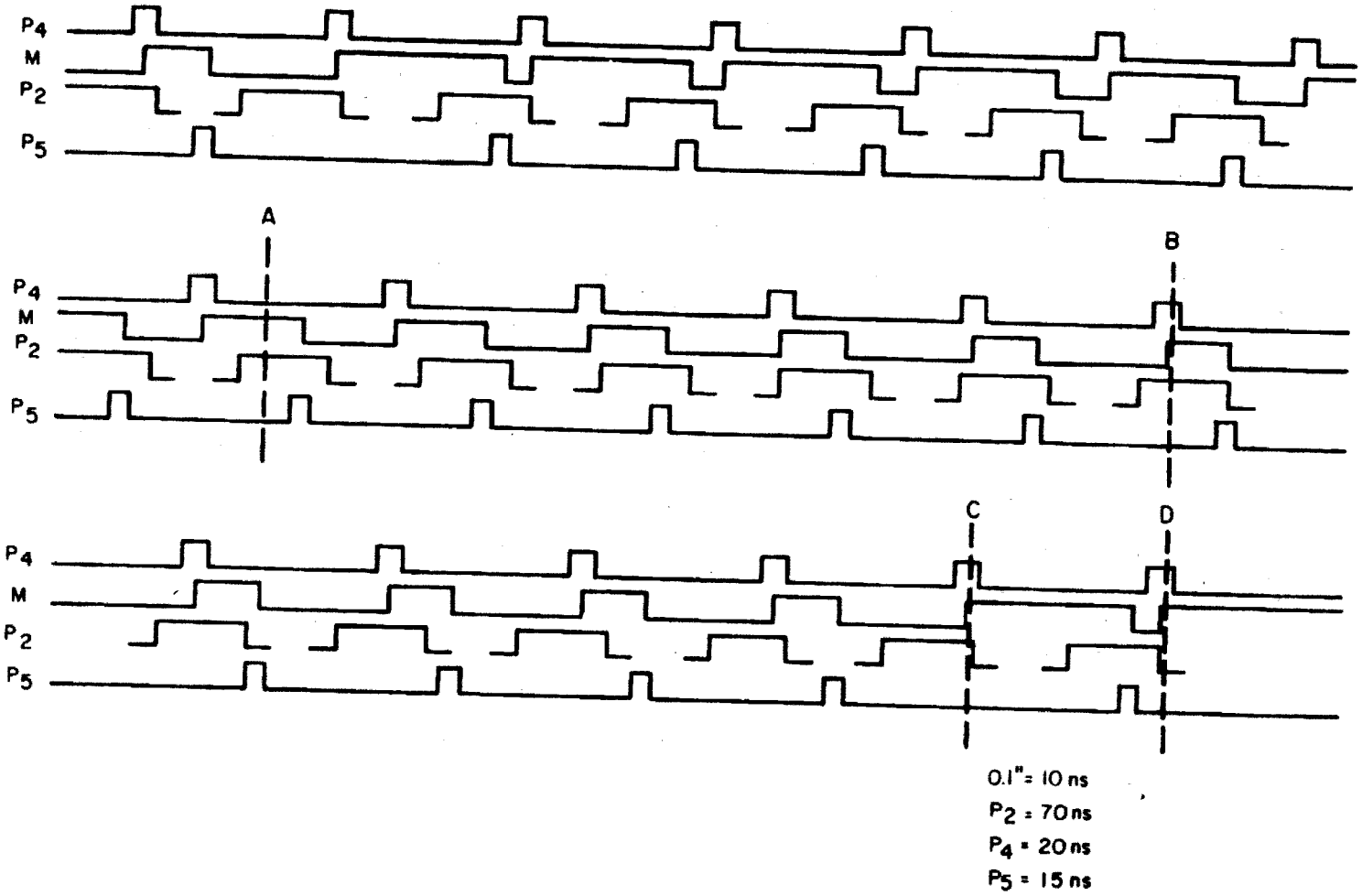

FIGURE 17 Timing Diagram (U)

For the first combination, in which P_2 follows the memory, the inhibit is set immediately upon the occurence of P_2. In this case, P_5 will occur a fixed time later, dependent on the propagation delay through the transfer gate and the inhibit logic, and reset the memory.

For the second case, in which P_2 precedes the setting of the memory, the inhibit will be set immediately following the setting of the memory, provided the P_2 pulse is still present. If the P_2 pulse is past, the condition reverts to the first combination where P_2 occurs after the memory has been set.

Point C indicates the situation where the coincidence of P_2 with the memory is not of sufficient duration to produce a pulse long enough to be propagated. This case also reverts to the first combination. Also at Point C there is no information in the memory to be transferred to the inhibit and a pulse will be allowed to reach the output.

Referring to Figure 18, the critical pulses are P_2, P_4, and P_5. The relationships between these pulses are as follows:

(a) P_5 = minimum recognizable pulse width*

(b) $P_2 = P_5 + \Delta t_p$**

(c) $P_4 = P_5 + 5$ s

Typical values are:

(a) t5 = 15 ns

(b) t2 = 70 ns

(c) t4 = 20 ns

(d) Δt_p = 50 ns

---

* As pulses become increasingly narrow, they reach a minimum width which will not be propagated through a gate. For the Sylvania SG220 series this width is about 10 ns.

** Δt_p is the sum of the propagation delays through the transfer gate, the inhibit logic, and the flip-flop in the memory logic.

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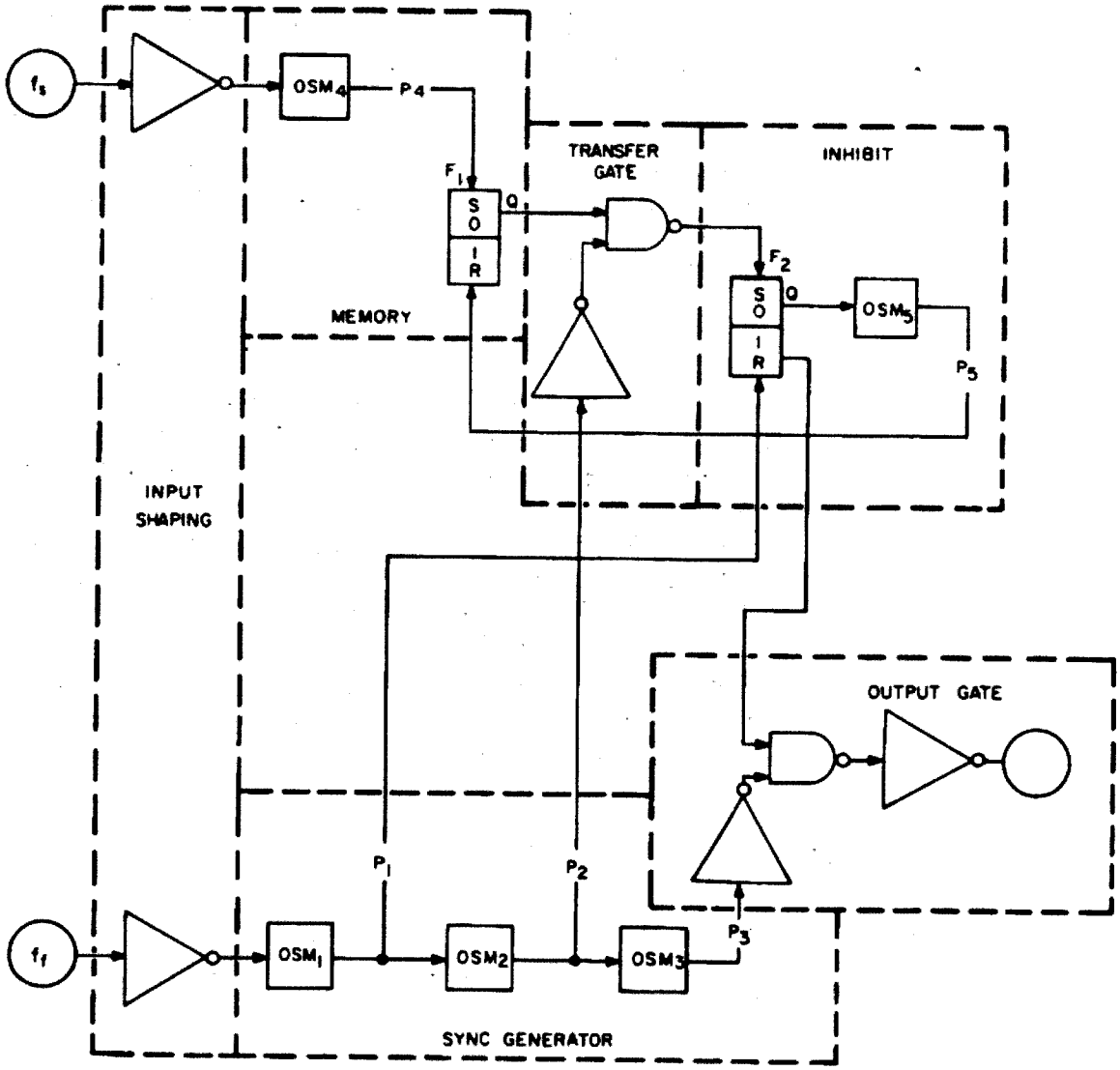

FIGURE 18 Pulse Subtractor Logic Diagram (U)

The three pulses, P_2, P_4, P_5 are of particular importance because of the possible race conditions that are normally associated with the gating of two asynchronous pulse trains. P_2 is a fixed width pulse that occurs at a fixed time after each f_f pulse and, therefore, represents the f_f pulse for the timing operation. P_4 also is a fixed width pulse but occurs immediately upon occurence of an f_s pulse. A P_4 pulse represents an f_s pulse.

The pulse width of P_2 is determined by the case as illustrated by Point D. Here, the memory has been set prior to pulse P_2 and P_2 is still present during the P_4 pulse. P_2 must be sufficiently long so that P_5 has finished before P_4. If P_5 finishes after P_4 then the memory will not be set and an extra count will result. P_2 therefore must be equal in width to pulse P_5 plus the propagation delay through the transfer gate, the inhibit, and the memory flip-flop to insure against the memory missing a pulse.

P_4 and P_5 need only to be long enough to be propagated. P_4 can be made slightly wider than P_5 to reduce the width of P_2.

(11) Timing in the Third Pulse Subtractor

In the third PS, if only one f_s pulse occurs between two f_f's, timing will be similar to the cases described in the previous section; therefore, the discussion will not be repeated.

Assume the condition that an f_s pulse has been stored in Memory I and another f_s arrives. The pulse is applied to Transfer Gate II which is controlled by the Q output of Memory I. The output from Q is applied through an 80 ns delay logic to the transfer gate and represents the command signal. When Q goes from a logic "0" to "1" the transfer gate is turned on after a delay of 80 ns. Since the pulse width of f_s is less

than 50 ns, the pulse will not be propagated through the gate if Memory I was not preset. This means that Transfer Gate II will be in an allowed state only when the second consecutive f_s pulse is applied at the input. Thus, the second f_s pulse will be passed through the transfer gate and will set Memory II. Memory II will provide an inhibit for the output gate and trigger a 30 ns monopulse element. This 30 ns pulse is fed to the reset inhibit gate and would reset Memory I if the gate would be in "allowed" state. However, the pulse from Transfer Gate II was also passed through a time delay logic to inhibit the reset pulse. The delay logic delays the trailing edge of the pulse (stretching the pulse) and effectively waits for the reset pulse to arrive at the inhibit gate. To function properly the pulse width of the inhibit should be greater than the propagation time through all the logic elements in the path of the reset pulse plus the pulse width of the reset pulse. If the above condition is satisfied, Memory I will not be reset; therefore, two f_s pulses will be stored in the pulse subtractor.

As the f_f pulse arrives, the sync generator produces three consecutive pulses. The first will enable Transfer Gate I to set Memory II but since it is already set, the pulse will have no effect. The second pulse is fed to the output but because of the presence of the inhibit function, an output pulse will not be generated. The third pulse from the sync generator will reset Memory II.

Memory I was not reset during this process because the only time a reset pulse is generated is when the Q output of Memory II changes states from logic "1" to "0" (that is, from reset to set) which did not occur.

After the above process f_s or f_f may occur. If f_s arrives first, Memory II will again be set as described. However, if f_f occurs first, the information from Memory I will be transferred to Memory II. An inhibit function will be generated and Memory I will

be reset since the reset inhibit function is not present. The third pulse from the sync generator will reset Memory II. Thus, both storage elements are now in reset state.

If both pulses f_f and f_s occur at the same time, the f_f pulse may arrive at the output gate before the inhibit function is generated. This would produce an output and also reset both memories resulting in an error. To prevent the above, a time delay of 20 ns is introduced between the second monopulse circuit of the sync generator and the inhibit gate.

(12) Monostable Elements

The success of the pulse subtractor is largely due to a successful attempt to fabricate an extremely high speed narrow pulse width monostable multivibrator. Rise and fall times on the order of 5 ns were achieved as well as pulse widths of less than 10 ns.

Figure 19 represents one monostable configuration. This configuration combines one flip-flop with two gates to provide a very fast monostable which responds to the falling edge of a pulse. The flip-flop is connected in such a way that the falling edge of a pulse caused Q to go to zero. The zero is propagated through the gates and resets the flip-flop. The pulse width of the monostable is approximately equal to the total propagation time of the gates. This configuration does not readily lend itself to long pulse widths nor is it easily adjusted to a specific pulse width.

Figure 20 represents a second monostable configuration and requires two gates, a diode, and a capacitor. This monostable responds to a positive dc level and yields pulse widths as short as 6 ns. The pulse width of the monostable configuration of Figure 20 is proportional to the delay in G_1 and can therefore be controlled. The addition of a capacitor and diode provide this control.

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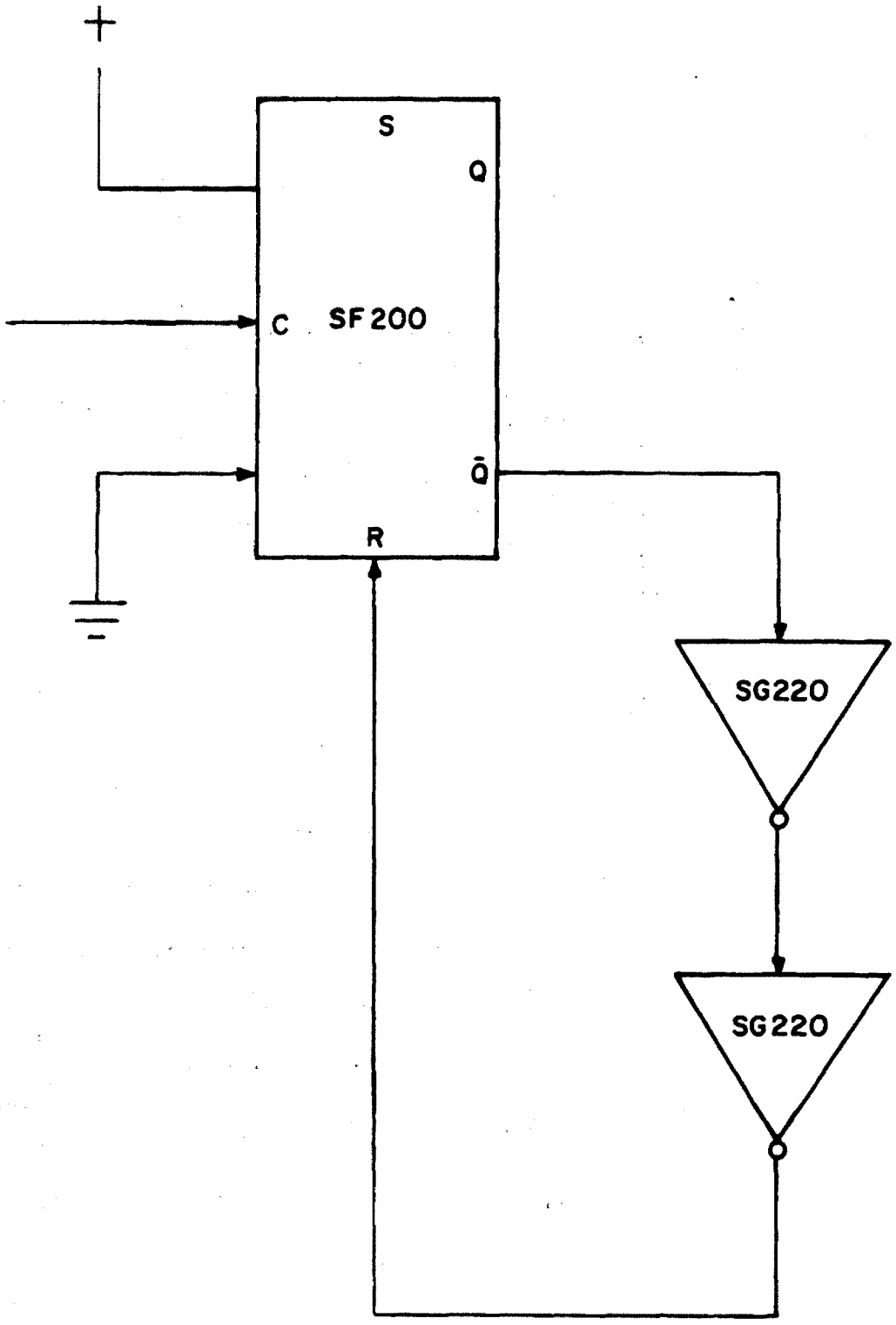

FIGURE 19 Monostable Multivibrator (U)

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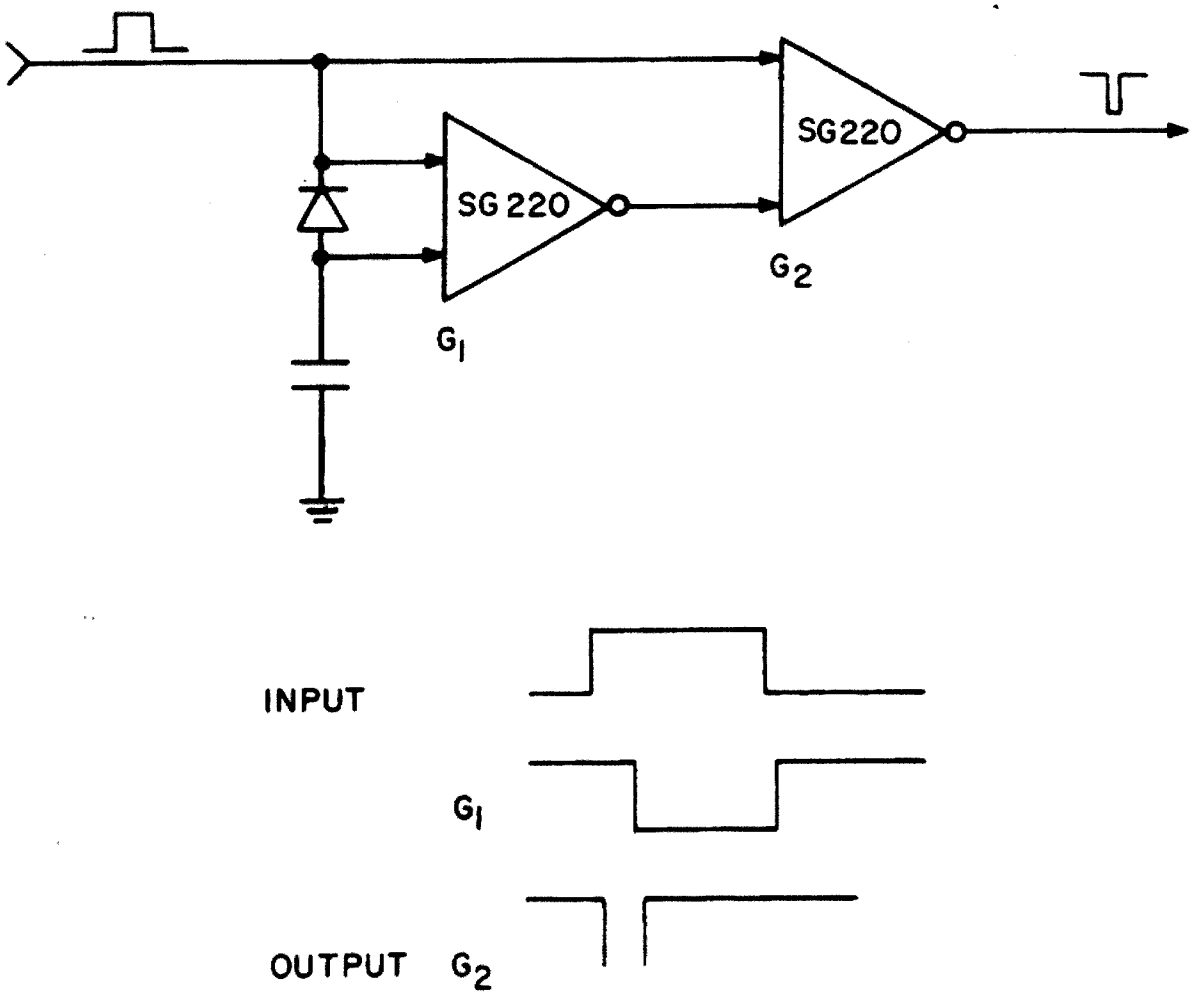

FIGURE 20 Monostable Multivibrator (U)

e. Zero Beat Detector (Figure 21)

The accuracy of the calibration scheme, in part, relies on the ability of the operator to tune an external oscillator to the third IF frequency. The zero beat detector is a tuning aid which enables the operator to tune a beat oscillator to within 1 Hz of the third IF frequency.

Consisting of a double balance mixer, a high gain amplifier, and a set of earphones, the zero beat detector mixes the external oscillator frequency with the third IF and amplifies the resulting difference. As the external oscillator is tuned to approach the frequency of the third IF, the output frequency approaches a null (zero beat). Since the amplifier is of the saturating type, frequencies which are normally below the range of hearing are still audible. Thus, the operator is able to tune the oscillator very close to the true null.

f. Oscillator

Because there is generally modulation associated with the third IF frequency, a separate oscillator, tuned to the IF frequency, is used to inject the IF frequency into the pulse subtractor. The oscillator has a center frequency of 455 kHz and is tunable over a band of 450 to 460 kHz. Tuning is accomplished by means of a 10 k Ω potentiometer.

The oscillator is a vendor item purchased from Greenway Industries, Inc.

Variable Frequency L-C Oscillator
Model #L-263-1
Quotation #L-263-1-6833

g. Oscillator Buffer (Figure 22)

The oscillator buffer prevents loading of the oscillator and provides isolation between the pulse subtractor and the zero beat detector.

The input stage of the oscillator buffer is an emitter follower (Figure 13). The emitter follower drives two separate amplifiers; the first outputs to the mixer, the second outputs to the pulse subtractor.

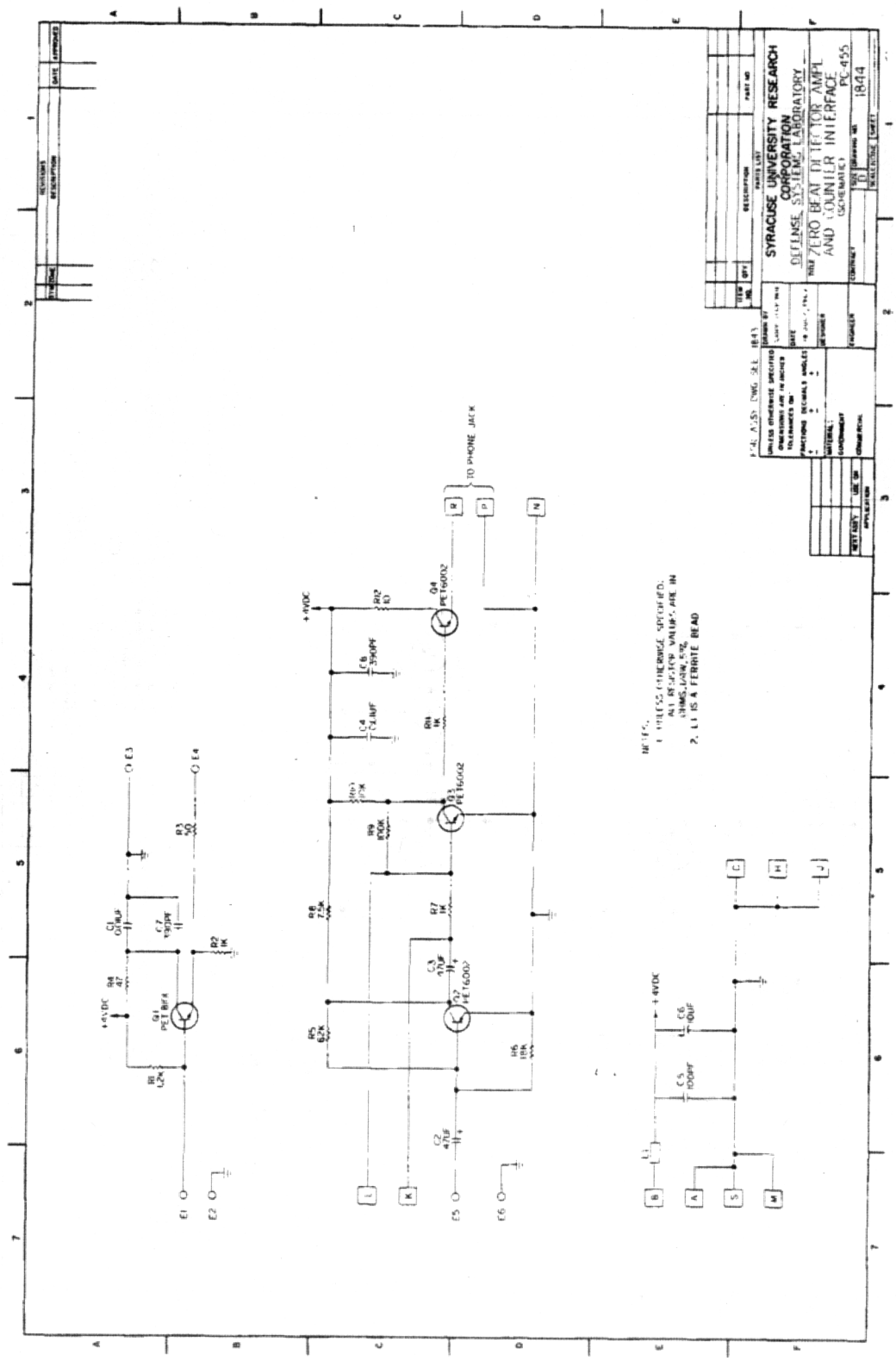

FIGURE 21 Zero Beat Detector Amplifier and Counter Interface (U)

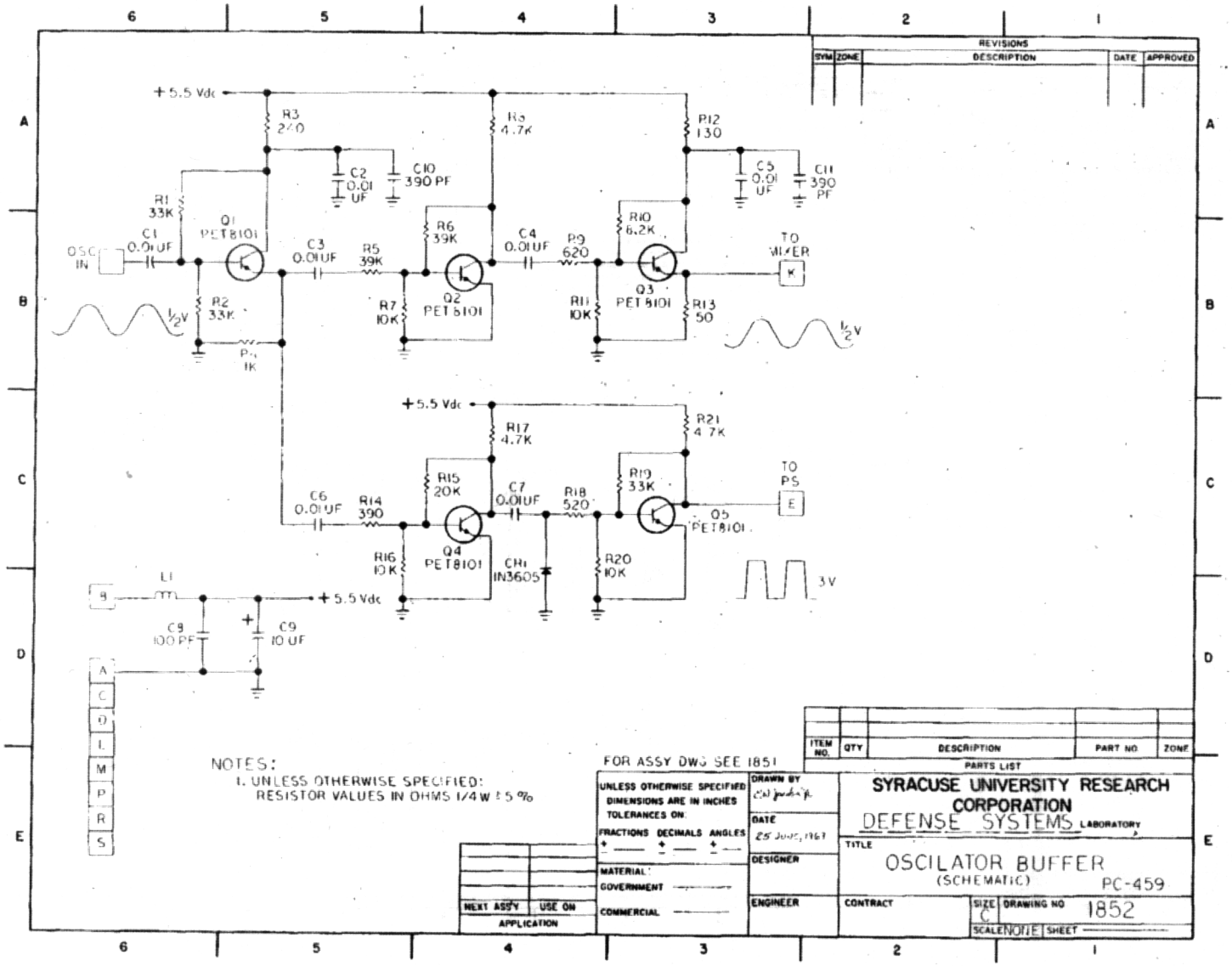

FIGURE 22 Oscillator Buffer (U)

As the sole function of the first amplifier is to provide isolation to the mixer, the overall gain is approximately one. The last stage has an output impedance of 50 ohms to match the input impedance of the mixer. The second amplifier provides high gain as well as isolation to the pulse subtractor.

h. Counter Interface (Figure 21)

The counter interface is an emitter follower used to drive the counter. The 50 ohm series resistor in the output of the circuit provides damping to subdue ringing on the counter input.

i. Counter[1]

To obtain the input frequency, the output of the third pulse subtractor must be counted over a one second period. This is accomplished through the use of a general purpose counter. The Hewlett Packard Model 5216A was chosen because of its small size, lightweight, and stability. It also has the added feature of having a digital output which enables the display to be remote.

j. Power Supply[2]

The calibrator requires a single dc source of 5.5 V and is provided by a Power Design Model UPMD-6 Modular Power Supply.

Important specifications are listed as follows:

(1) Input 115 volts ±10%, 57 to 63 Hz

(2) Regulation better than 0.01% + 2 mV

(3) Ripple plus noise -- less than 1 mV peak to peak

(4) Stability -- 1 mV per 8 hours

(5) Operating temperature -- 0° C to 50° C

(6) Source impedance -- 1 ohm at 1 MHz

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1 "Electronic Counter 5216A, Operating and Service Manual", Hewlet Packard, June 1968.

2 "Redule Modular Power Supplies", Model UPMD-6, Power Designs, Inc.

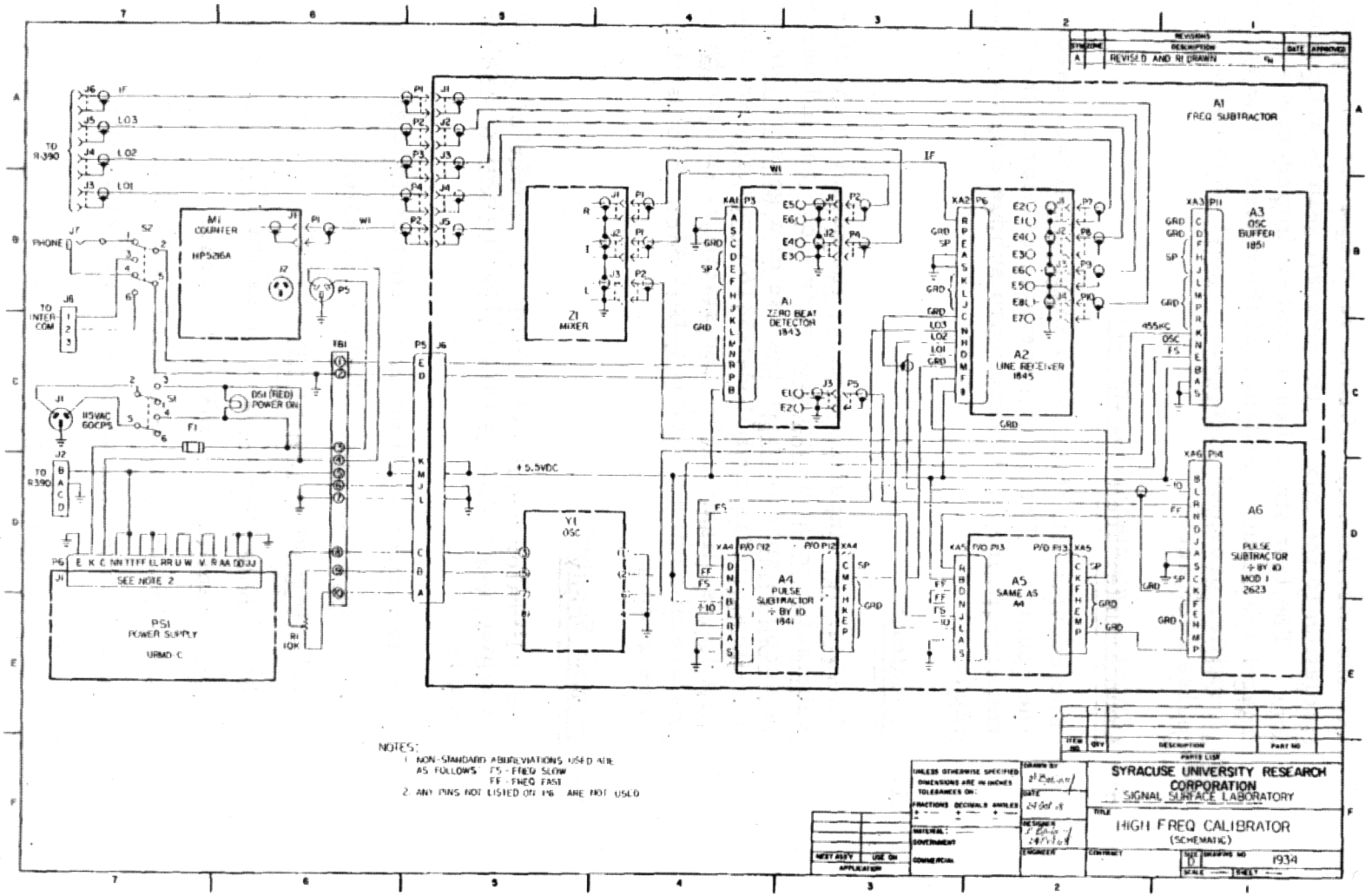

FIGURE 23 Wiring Diagram of R-390A/URR Digital Frequency Readout Unit (U)

SECTION IV

TEST RESULTS AND CONCLUSIONS

To determine the accuracy of the SURC designed R-390A Frequency Readout Unit, a calibration test was performed using an RF generator and the HP 5245L Frequency Counter. The average error as read from the meter was 17 Hz. Taking into account that the last digit displayed on the meter is 10 Hz units and that the accuracy of the display unit is ± 1 last digit (±10 Hz), the RF input frequency to the receiver may indeed be accurately determined. As a comparison, the dial reading of R-390A showed an average error of 2.920 kHz.

In conclusion it may be said that the accuracy of frequency readout has been greatly improved (170 times), the dial accuracy of the receiver is not important and the display of the readout has been improved.

The principle of this type of frequency readout may be applied to other receivers; however, the upper frequency range may not exceed 100 MHz. This limitation is due to the fact that integrated circuits are not available (at present) which operate reliably above 100 MHz.

SECTION V

OPERATING PROCEDURE

1. RECEIVER CALIBRATION

a. Tune receiver to known frequency
WWV -- 15.000,000 MHz

b. Tune the calibrator oscillator for a zero beat

(1) The calibrator now displays the frequency to which the receiver is tuned

(2) The zero beat detector will null when the receiver is tuned exactly on any signal frequency

2. SIGNAL FREQUENCY CALIBRATION

a. Used to quickly determine the frequency of the signal of interest.

b. Tune receiver to signal of interest; it is not necessary to tune the receiver exactly.

c. Tune the calibrator oscillator for a zero beat; the display will indicate the exact frequency of the incoming signal.

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13 ABSTRACT

The design and development of the R-390A/URR Digital Frequency Readout Unit is presented ~~in this report~~. The history of development including the techniques considered are discussed. Digital pulse subtraction, which was chosen as the most economical technique, is described in detail.

The new approach to frequency readout ~~presented utilizes~~ uses the existing local oscillators of the receiver and, by a pulse subtraction process, extracts the input frequency of the receiver with an accuracy of ±20 Hz. (plus or minus)

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14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Frequency Subtraction by Digital Technique						
Divide-by-10 Logic						
Pulse Subtractor						
Monostable Multivibrator						